別紙様式３

学位論文の要旨

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学位論文 題　　目	Research of Low Voltage CMOS Current Mode Reference Circuit Based on Subthreshold Operation (弱反転動作に基づく低電圧 CMOS 電流モード基準発生回路の研究)

【論文の要旨】（和文の場合 1,200 字程度、英文の場合 800 語程度）

Recent mobile devices are equipped with various very-large-scale integration (VLSI) which integrates the analog circuits such as the reference circuit (REF), power management unit (PMU), analog-to-digital converter (ADC) in a single chip. These analog circuits in VLSI are strongly required low power (low voltage) operation to extend system lifetime or battery life. In addition, each analog circuit in VLSI always needs several reference voltages and/or currents suitable for each circuit. The reference voltages and currents are strongly required low sensitivity to variations in power supply voltage (VDD), temperature and process variations to maintain performance of each circuit. Hence, the reference circuit is one of the very important functional block in VLSI, and its important requirement is expandability such as multiple voltage and/or current outputs, selectable output value, high accuracy and small area. Bandgap reference (BGR) circuit is well known and has been widely used as the reference circuit. Generally classifying, the reference circuits are categorized three architectures which are voltage mode, current mode and resistor-less architectures. Above all, since the current mode architecture has aforementioned expandability, it is suitable as the reference circuit in VLSI. However, prior current mode circuits have not enough realized low power, low voltage operation and small area.

In this thesis, novel current mode reference circuit is proposed and compared to conventional circuits. Chapter 1 presents the background information and general overview of reference circuit along with design requirements, development history, classification and design issues of circuit architectures. By comparing figure of merit (FoM), it has revealed that the current mode architecture is not effectively utilized despite it has excellent expandability.

Chapter 2 shows the circuit topology, operation principle and simulation results of proposed novel low voltage current mode reference circuit. The proposed circuit is designed with the subthreshold design technique and has unique structure that is regarding the proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) generators as two stage operational amplifier. The design methodology is shown by theoretical analysis. The proposed circuit is designed and simulated by using 65 nm CMOS process device parameters, and the low voltage operation performances from 0.6 V power supply voltage are demonstrated. Furthermore, FoM of proposed circuit is improved more than ten times compared with prior current mode circuits.

Chapter 3 shows the measurement results of the actual silicon chip by using 0.6 μm CMOS process. Although the temperature coefficient and the output voltage value show discrepancy from the simulation result, the characteristics can be adjusted by trimming function. From this measurement results, the effectiveness of trimming functions is demonstrated.

In Chapter 4, the performance improvement method by using self-regulator and novel adaptive biasing technique is proposed, and its effectiveness is demonstrated by simulation with 65 nm CMOS process device parameters. The self-regulator provides the optimized voltage which is adaptively following process, voltage and temperature (PVT) conditions of the reference circuit core by adopting the proposed adaptive biasing technique. In the improved circuit, the line sensitivity, temperature coefficient and power supply rejection ratio are improved with maintaining lower minimum required supply voltage about 0.8 V. As the result, FoM of improved circuit is improved about ten times compared with prior proposed current mode circuit.

Finally, Chapter 5 concludes this thesis and future work.

（注１） 論文博士の場合は、「専攻、入学年度」の欄には審査を受ける専攻のみを記入し、入学年度の記入は不要とする。

（注２） フォントは和文の場合 10.5 ポイントの明朝系、英文の場合 12 ポイントの times 系とする。

（注３） 学位論文題目が外国語の場合は日本語を併記すること。

（注４） 和文又は英文とする。