Design and Analysis of Low-Power Low Dropout Regulator without Op-Amps

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Abstract

Conventional Low Dropout (LDO) regulator that the difference between input and output voltages is controlled by an operational amplifier (op-amp) in continuous time requires a static steady-state current and phase compensation in the feedback path. In addition, it is difficult to use low-supply-voltage because it is difficult to operate general op-amp at low-voltage. In this paper, new LDO regulator is presented to solve the above problems. The proposed LDO regulator can be operated at low-voltage and low-power-consumption because the proposed LDO regulator is no need op-amps. Furthermore, the phase compensation circuit is not needed. The proposed LDO regulator was simulated using SPICE simulator with Phenitec Semiconductor 0.6-μm CMOS process parameters. The simulation results show the proposed LDO regulator works as theory.

Keywords: Low dropout regulator, LDO, op-amp less, low power, low voltage

1. INTRODUCTION

Recently, portable devices such as smart phones become smaller and smaller and various functions are implemented in the devices by virtue of very fine semiconductor technology [1]–[4]. Since the portable devices are driven by a battery, the power supply circuits such as DC-DC converter and low dropout (LDO) regulator are very important [5]–[8]. Especially, one of the most important characteristics of these circuits is efficiency because the energy of the battery is limited [8]. Therefore, many researchers try to research about high efficiency power supply circuits [5]–[8].

The regulator is classified in Linear Regulator and Switching Regulator. The linear regulator means LDO regulator which can be realized by a simple circuit using op-amp. In many cases, LDO has very small ripple and outputs very stable-state voltage, therefore, LDO regulators are used widely [1], [2]. However, almost all of the LDO regulators require an operational amplifier (Op-Amp) as the error amplifier. Therefore, it is difficult to reduce the power consumption of the LDO regulator, as the results, efficiency of them are low. In addition, low-voltage operation of the LDO regulator is also difficult because Op-Amp require the relatively high supply voltage.

In this paper, we propose a novel op-amp less LDO regulator. The proposed LDO regulator consists of hysteresis comparator and digital circuit components, and no need Op-Amp. Therefore, very low power consumption and low-voltage operation can be expected. In this paper, the simulation results and effectiveness of the proposed LDO regulator is shown. This paper consists of 5 chapters. Chapters 2 and 3 describe the conventional and the proposed LDO regulators, respectively. Simulation results are presented in Chapter 4. Lastly, the conclusion and future work are shown in Chapter 5.

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2. CONVENTIONAL LDO REGULATOR

Basic architecture of the conventional LDO is shown in Figure 1. The operation principle is as follows. Voltage of the non-inverting terminal of the op-amp becomes same as the voltage of reference voltage source (V_{REF}) by the virtual short characteristics of the op-amp. The output voltage (V_{out}) is derived by the resistance values of R_1 and R_2.

$$V_{out} = \left(\frac{R_1 + R_2}{R_2}\right) V_{REF} \tag{1}$$

However, this LDO regulator consumes the relatively high power because this LDO regulator requires an op-amp which consumes the static current. Furthermore, in this LDO regulator, there is a feed-back path through the op-amp, therefore phase compensation is necessary in order to prevent an oscillation of the LDO circuit. In many cases, we employ a capacitor and a resistor as the phase compensation circuit

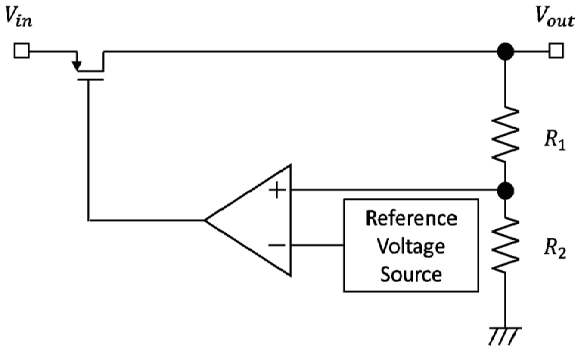

Figure 1 The circuit diagram of the conventional LDO regulator.

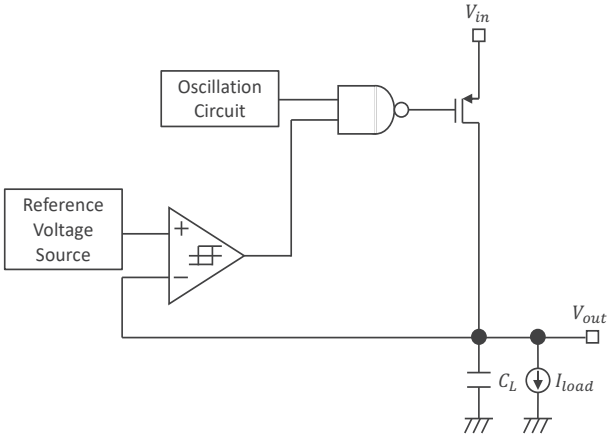

Figure 2 The circuit diagram of the proposed LDO regulator.

in the feed-back path. In this case, chip area for LDO regulator is increase. This means the increase of the cost.

3. PROPOSED LDO REGULATOR

In this chapter, overview of the proposed LDO regulator. The architecture of the proposed LDO regulator is explained firstly.

3.1 Architecture of the Proposed LDO Regulator

Basic architecture of the proposed LDO regulators is shown in Figure 2. This circuit consists of a hysteresis comparator, a reference voltage source, an NAND gate, PMOS transistor for drivers and an oscillation circuit. The C_L and I_{load} are a load capacitance and a load current source, respectively. In this architecture, since the op-amps are not required, the static current consumption can be reduced drastically. Furthermore, when the load capacitance is relatively small, power transistor (PMOS transistor) tunes OFF, so that current consumption can be reduced. That is to say, the power transistor behaves like the switching ON and OFF. As mention previously, the proposed LDO regulator is no need op-amps, it can be operated under low supply voltage and the phase compensation circuit. Figure 3 shows the theoretical output waveform of the proposed LDO regulator. When the output voltage, the high threshold voltage and the low threshold voltage of the hysteresis comparator are respectively defined by V_{out}, V_{refH}, and V_{refL}, the proposed LDO regulator operates as follows.

When $V_{out} \leq V_{refL}$, the pulse signal from the oscillation circuit is inputed into the gate of the PMOS transistor through the NAND gate. When pulse signal is high, the electrical charge is supplied from input through the channel of the PMOS transistor, and then V_{out} is increased. Wnen $V_{out} > V_{refH}$, the pulse signal from the oscillation circuit is stopped by NAND gate, and then V_{out} is decreased. The waveform of $T_{recover}$ and T_{hold} are repeated as shown in Figure 3. (T_{hold} is defined as the time when V_{out} is decrease from V_{refH} to V_{refL} and $T_{recover}$ is defined as the time when V_{out} is increase from V_{refL} to V_{refH}.)

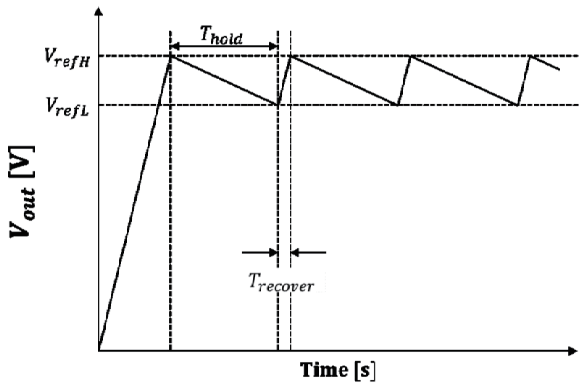

Figure 3 The theoretical output waveform.

3.2 Theoretical Analysis of the Proposed LDO Regulator

In the proposed LDO regulator, the ripple of V_{out} depends on the hysteresis width of the hysteresis comparator. In this section, theoretical analysis based on some parameters is clearly.

Figure 4 shows the theoretical output waveforms in $T_{recover}$ shown in Figure 3. The Figure 4(a), 4(b), 4(c) and 4(d) are the pulse signal generated by oscillation circuit, the waveform of the output voltage, the current waveform in PMOS transistor, and the current waveform of load current source. The out-

put current (I_{out}) of PMOS transistor decreases by the internal resistance R_{on} and C_L. The decrement depends on R_{on} and C_L which is the time constant. When the period of the pulse signal sets small enough for the time constant, I_{out} can be approximated by a constant current pulse [2]. In this way, I_{out} can be given by

$$I_{out} = \frac{V_{in} - V_{out}}{R_{on}} \tag{2}$$

where V_{in} is the input voltage of the proposed LDO regulator. The electric charge supplied by the PMOS transistor in one period of the clock ($\Delta Q_{recover}$), and the electric charge discharged by I_{out} (ΔQ_{load}) are expressed as follows using principle of conservation of charge.

$$\begin{aligned} \Delta Q_{recover} &= I_{out} \times \frac{T_{CLK}}{2} \\ &= \frac{V_{in} - V_{out}}{R_{on}} \times \frac{T_{CLK}}{2} \end{aligned} \tag{3}$$

$$\Delta Q_{load} = I_{load} \times T_{CLK} \tag{4}$$

The voltage which is boosted during one period of the pulse signal (ΔV_{cycle}) can be given as follows from principle of conservation of charge.

$$\begin{aligned} \Delta V_{cycle} &= \frac{1}{C_L}\left(\Delta Q_{recover} - \Delta Q_{load}\right) \\ &= \frac{T_{CLK}}{C_L}\left(\frac{V_{in} - V_{out}}{2R_{on}} - I_{load}\right) \end{aligned} \tag{5}$$

When V_{hys} is defined as the hysteresis width, and N_{cycle} is defined as the number of necessary switching time to increase the voltage which is equal to V_{hys}, V_{hys} can be expressed as follows.

$$\begin{aligned} V_{hys} &= N_{cycle}\Delta V_{cycle} \\ &= \frac{N_{cycle}}{C_L f_{CLK}}\left(\frac{V_{in} - V_{out}}{2R_{on}} - I_{load}\right) \end{aligned} \tag{6}$$

where f_{CLK} is clock frequency of pulse signal. From Equation (6), V_{hys} of the proposed LDO regulator can be determined by f_{CLK} and C_L.

4. SIMULATION RESULTS

The operation and performance of the proposed LDO regulator were confirmed by using SPICE simulator with the model parameter of the Phenitec semiconductor 0.6μm CMOS process. The detailed circuit diagram of the comparator which is used for this simulation is shown in Figure 6. Figure 5 shows the circuit diagram of the comparator used in the hysteresis comparator shown in Figure 6. Table 1 shows the design values of Figures 5 and 6.

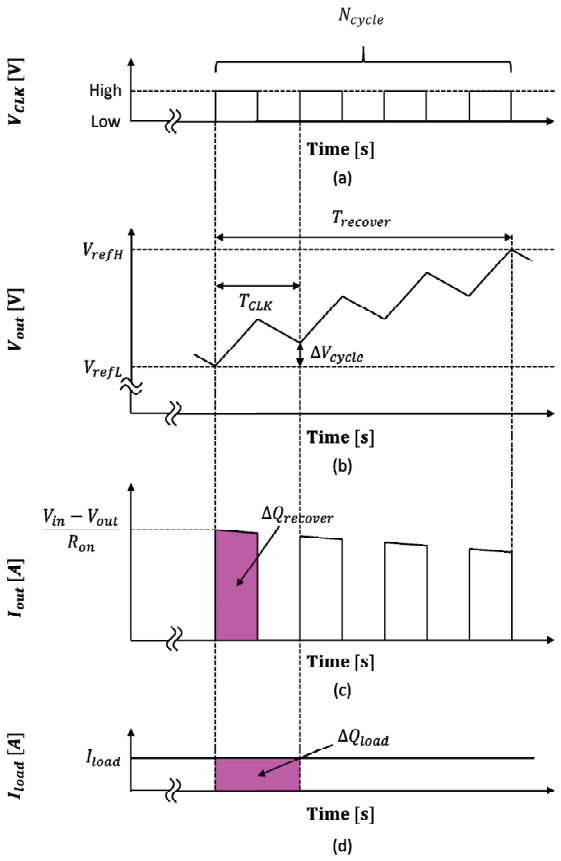

Figure 4 The output waveform of theoretical $T_{recover}$.

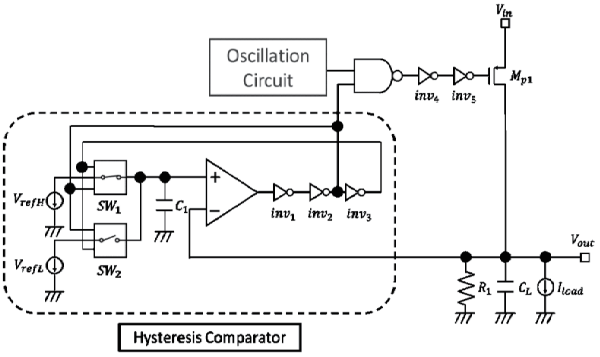

Figure 5 The Detailed architecture of the proposed LDO regulator for simulation.

Figure 7 shows the result of the transient analysis. From this figure, we can confirm that the values of V_{refH} and V_{refL} are well accorded with the theoretical values. Figure 8 shows the enlargement of V_{out}. From the theoretical ΔV_{cycle} is 2 mV however, simulation results is 21 mV, that is to say, the simulation results of ΔV_{cycle} are not accorded with the

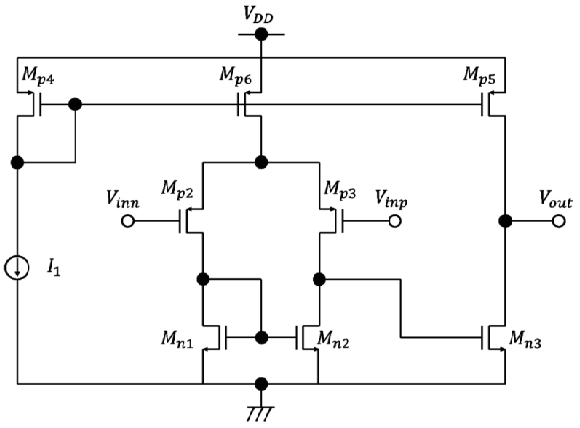

Figure 6 The circuit diagram of the comparator used in Figure 5.

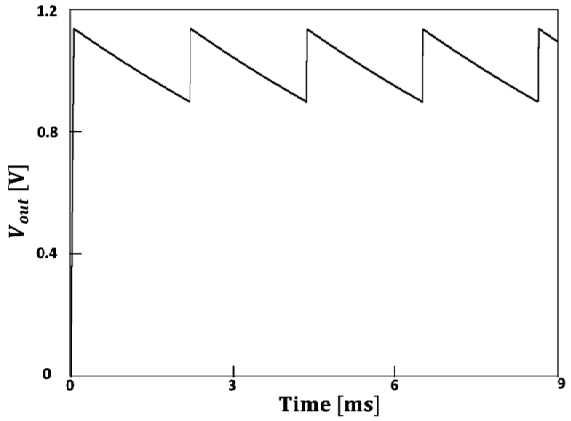

Figure 7 The simulated output waveform.

Table 1 Design Values of the Proposed LDO Regulator.

Items	Value
M_{p1} [μm/μm]	5.6/0.6 (4)
M_{p2} – M_{p5}[μm/μm]	21.5/4 (1)
M_{p6} [μm/μm]	5.6/0.6 (2)
M_{n1} – M_{n3} [μm/μm]	13/4 (1)
V_{in} [V]	2.0
I_1 [μA]	50
R_1 [MΩ]	1
I_{load} [μA]	0.1
C_L [nF]	10
f_{CLK} [MHz]	1

The number in ( ) means the number of the MOS transistors connected in parallel.

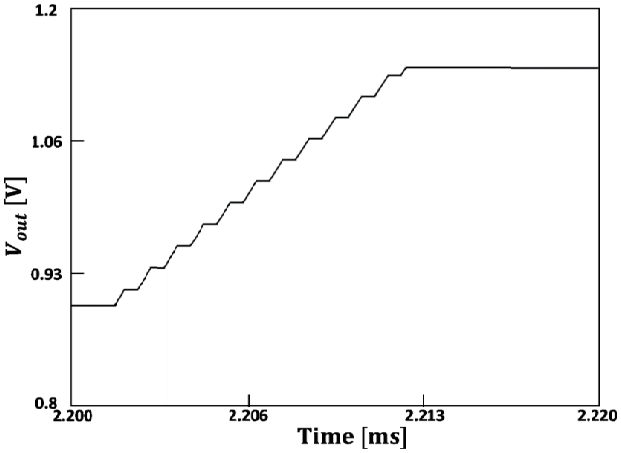

Figure 8 The output waveform to confirm $T_{recover}$.

Table 2 The Power Consumption of the Proposed and Conventional LDO Regulators.

Condition	Proposed [μW]	Conventional [μW]
$I_{load} = 0.1$ [μA]	198	264
$I_{load} = 1.0$ [μA]	235	265
$I_{load} = 10$ [μA]	245	265

theoretical ones. When we analyzed the circuit, I_{out} was treated as a constant current pulse, however, I_{out} is decrease by R_{on} an C_L in actuality. In an actual design, we must pay attention to this and the reduction of this difference is future work.

Table 2 shows the power consumption of the proposed LDO regulator. From this table, the power consumption of the proposed LDO regulator is smaller than that of the conventional one and is increase with the increase of I_{load}. This reason is ΔV_{cycle} is decrease and N_{cycle} is increase when I_{load} is increase. Therefore, the proposed LDO regulator is suitable for the application with small load current.

Lastly, the simulation results and theoretical values of the proposed LDO regulator is listed in Table 3.

5. CONCLUSION

In this paper, new low-power LDO regulator has been proposed and analyzed. It has better performance than the conventional LDO regulator, especially it has advantage of the power consumption becasue of no need Op-Amps. This could be confirmed through SPICE simulations, as the result, the power consumption was reduced when the light load. In addition, because it was designed by exclude op-amp part, the phase compensation circuit is not necessary. The ripple of the output voltage could be confirmed and according to the value of ΔV_{cycle}, the simulation result is not matched with the theoretical one. Since controlling ripple is difficult when ΔV_{cycle} becomes larger than V_{hys}. This problem should be solved for actual design, and this is the future work.

Table 3 Simulation Results and Theoretical Values of the Proposed LDO Regulator.

Items	Simulation	Theoretical
Average of V_{out} [V]	1	1
V_{refH} [V]	1.1	1.1
V_{refL} [V]	0.9	0.9
Ripple Width [V]	0.2	0.2
V_{cycle} [mV]	21	2

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