宮崎大学大学院

博士学位論文

Study on Battery-less Signal Conditioner for a Biological Signal Measurement System Using Smartphone

スマートフォンを用いた生体信号計測システムのための バッテリレスシグナルコンディショナに関する研究

2019 年 3 月

宮崎大学大学院農学工学総合研究科

物質・情報工学専攻

宮内　亮一

Abstract

In recent years, improving the quality of life and increasing the healthy life expectancy are becoming global concern and challenges. For this reason, management of health on a daily basis, and measuring the own vital data, such as heartbeats, pulses etc., using various equipment are essential. Wearable devices are well known one of the equipment for biological signal measurement system. However, the cost of these devices is often expensive, because these consist many functions that are realized by the display, storage, analog front end, cell battery and so on. The cell battery is one of the hardware, which prevents reducing the cost. On the other hands, energy harvesters often have a voltage rectifier circuit, which consists of active diodes with bulk regulation transistors and generates DC voltages from AC voltages. However, these diodes have the dead region, which does not ensure the stable operation of diodes(around -0.6 V to $+0.7$ V). For this reason, conventional voltage rectifier circuit cannot generate expected DC voltage.

In order to overcome these problems, we propose battery-less signal conditioner and new active diode with bulk regulation transistor and its application to the voltage rectifier circuit. Firstly with the proposed signal conditioner consists of an instrumentation amplifier, a filter and a voltage rectifier circuit. The proposed signal conditioner positively uses some functions of smartphone. The biological signal, sensed by using sensor, is converted to the digital data through the microphone terminal with A/D converter in the smartphone. And, the proposed signal conditioner is supplied the power through the earphone terminal of the smartphone. For this reason, the proposed signal conditioner not require the battery

in own device. In addition, the microphone input and the earphone output can use at the same time by using control software of smartphone, which parallelized processing of the earphone output and the microphone input. The proposed signal conditioner was verified through the measurement of surface electromyogram using discrete parts and smartphone (iOS). As a result of evaluation, the proposed system was operating correctly. The proposed active diode with bulk regulation transistor can eliminate the dead region by using a control signal from the comparator, which construct active diode. Next, we apply the proposed active diode with bulk regulation transistor to the integrated voltage rectifier circuit. The proposed active diode with bulk regulation transistor and voltage rectifier circuit were fabricated using a 0.6 μm standard CMOS process. From experimental results, the proposed active diode with bulk regulation transistor eliminates the dead region perfectly, and the proposed voltage rectifier circuit generates $+2.86$ V (positive side) and -2.70 V (negative side) under the condition that the amplitude and frequency of the input sinusoidal signal are 1.5 V and 10 kHz, respectively, and the load resistance is 10 kΩ.

Contents

List of Figures

List of Tables

Chapter 1

General Introduction

In recent years, improving the quality of life and increasing the healthy life expectancy (HALE) are becoming global concern and challenges [1] – [13]. The HALE is the time span that we can live without own health problems. Additionally, Japan is one of the longevity society in the world. However, there is the discrepancy between the life expectancy and HALE is about 9 years for male and 13 years for female [3]. Promoting own health and preventing the lifestyle-related disease are effective for decreasing this discrepancy [4]. For this reason, management of own health on a daily basis is very important, and measuring the own vital data, such as heartbeats, pulses etc, using various equipment are essential. The biological signal measurement system has a two categories such as the stationary type and the wearable type. In generally, Advantage of each measurement systems are known as follows; the stationary type has the high accuracy, real time measurement and multi channel, the wearable type (by using wearable devices) has the convenience and daily use. Especially, the wearable devices, which evolves at a rapid pace, are one of the equipment to measure the biological signal. In the future, own health management would become almost equal to management by personal trainers by analyzing measured data using artificial intelligence (AI) and deep learning [14][15]. However, it is difficult to realize the above system because the system requires the many functions

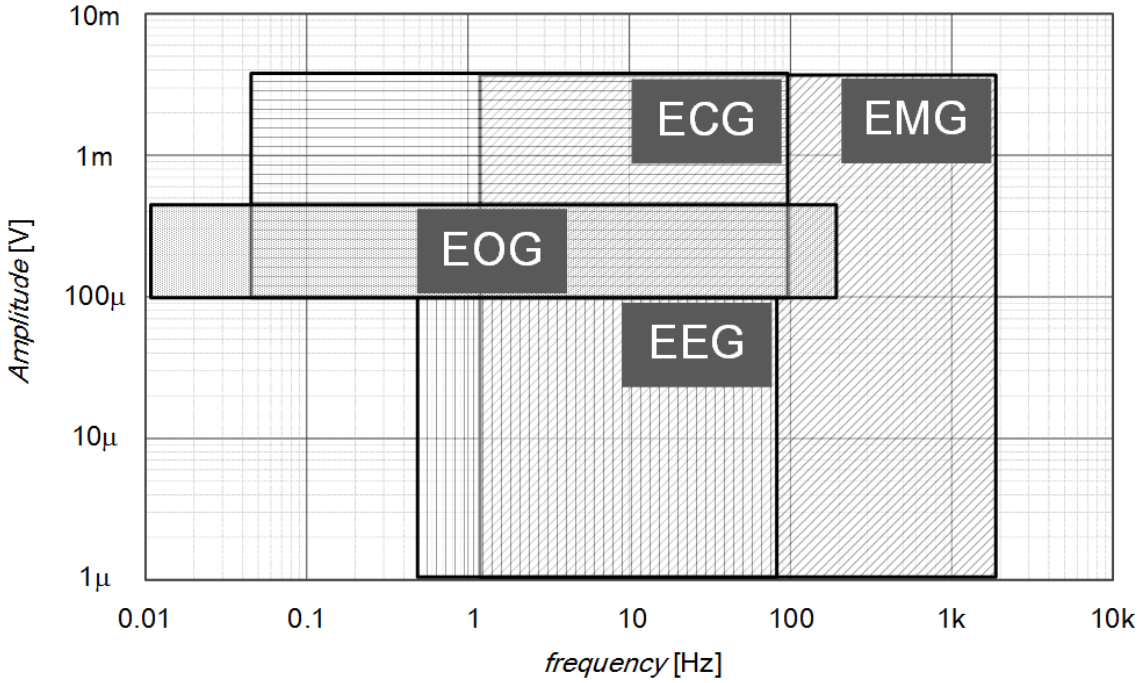


Figure 1.1: Characteristic of Biological Signal

and the cost will become high. Therefore popularization of the wearable devices is delayed.

Biological signals, such as Electromyogram (EMG), Electrooculogram (EOG), Electroencephalogram (EEG), Electrocardiogram (ECG), are well known as the vital data. In general, biological signals have characteristics of small amplitude (μV to mV) and low frequency range (DC to few KHz) shown in Fig. 1.1 [16]. In order to implement the biological signal measurement system, not only an analog circuit such as the amplifier, filter, Analog to Digital (A/D) converter, but also a digital circuit such as processor and memory are required.

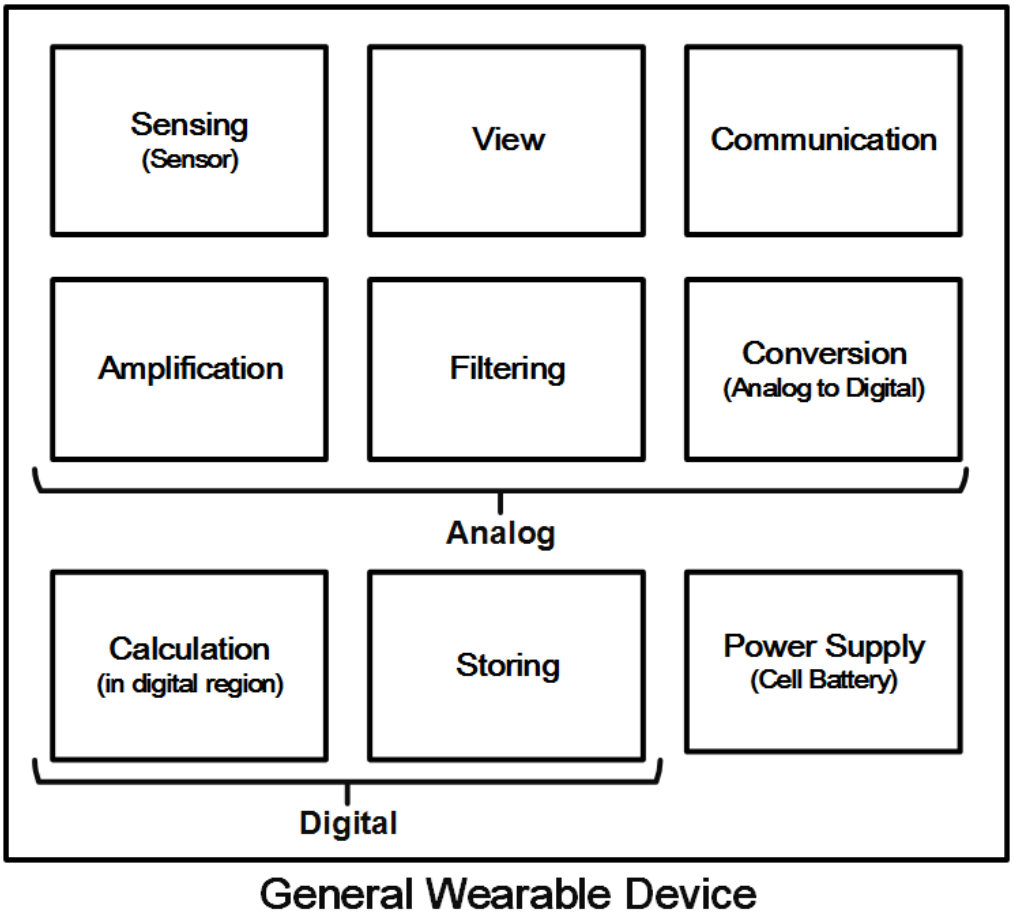
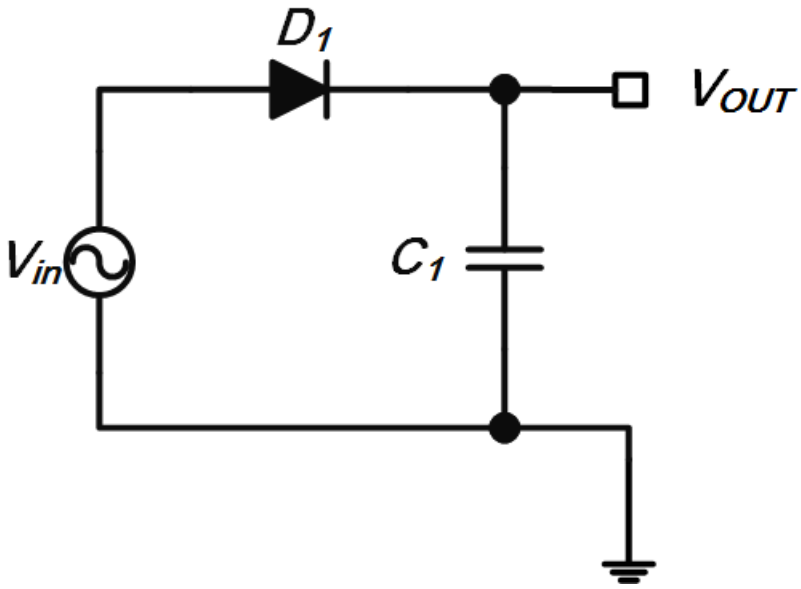


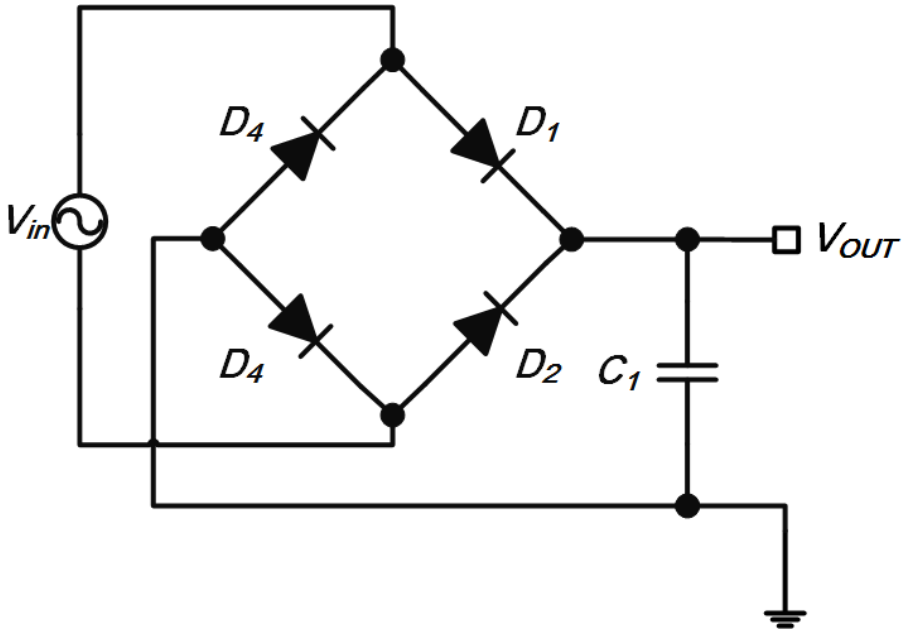
Figure 1.2: Function Block of General Wearable Device

In addition, the general wearable devices are consists of many function, such as the sensing, the view, and etc. shown in Fig. 1.2. That is to say, these kind of systems become complex and high cost. Especially, the cell battery is one of the hardware, which prevents reducing the cost. Therefore, omitting the cell battery is one of the effective approaches for reducing the cost.

Our research goal is achieving the simple measurement system, which is consist of sensor, signal conditioner and popularization equipment (smartphone). And this system will be going to measure the various signals by plug-and-play. Firstly, we propose new architecture of biological signal measurement system by using a smartphone and new signal conditioner for achieving the simple and low cost measurement system.



(a) Half-Wave Voltage Rectifier Circuit



(b) Full-Wave Voltage Rectifier Circuit

Figure 1.3: Figures-ABC.

The energy harvesters well known have a voltage rectifier circuit by using diodes shown in Fig. 1.3 [21] - [28]. In the voltage rectifier circuit of integrated energy harvesters, diode consists of parasitic diode of metal oxide semiconductor field effect transistor (MOSFET). In generally, the parasitic diode of MOSFET has a potential barrier

which is approximately 0.7 V, and it causes decreasing the generated voltages of voltage rectifier circuit. Therefore, using parasitic diodes is difficult to apply for the low voltage applications. Furthermore, in the case of using the parasitic diodes of MOSFET, the bulk terminal of MOSFET should be connected to V_{SS} (or lowest voltages of the circuit), however, since the input of the parasitic diodes of MOSFET is sinusoidal signal in many cases, the polar of the input signal is changed every second. To overcome these problems, the active diode with bulk regulation transistors (BRT) was proposed [18] - [20]. Using the active diode eliminates the potential barrier of parasitic diodes of MOSFET and Using the BRT overcome connecting the bulk terminal of MOSFET. However, the conventional active diode with BRT has the dead region (around ± 0.7 V) that the output voltage is indeterminate value. Therefore, the leak current is occurred in the conventional active diode with BRT. As the results, the performance of the application circuit using the conventional active diode with BRT such as the operation range, current consumption etc. degrades.

Next, we propose new active diode with BRT and its application to integrated voltage rectifier circuit. The proposed active diode with BRT can be realized adding an inverter to conventional one and has no dead region. And we propose the new integrated voltage rectifier circuit using the proposed active diode with BRT.

The thesis consists of four chapters. **Chapter 1** gives a general introduction to this thesis. This chapter describes general overview of biological signal measurement, problem of the biological signal measurement system and problem of the voltage rectifier circuit based on the active diode with BRT by using energy harvesting circuit. **Chapter 2** gives the proposed biological signal measurement system and the new signal conditioner. The proposed biological signal measurement system consists discrete parts and tests through the measurement of surface EMG (s-EMG). And experimental results and comparison result are described. **Chapter 3** gives the proposed active diode with BRT and its application to half-wave voltage rectifier circuit based on voltage doubler. The dead region of conventional and proposed active diode with BRT evaluate through the experiment by us-

ing actual chip which fabricated through the 0.6 μ m CMOS process. And its application to half - wave voltage rectifier circuit based on voltage doubler evaluated simulation and experiment by using the 0.6 μ m CMOS process. Finally, conclusion of my thesis and a discussion of future work are presented in **Chapter 4.**

Chapter 2

Signal Conditioner for Biological Signal Processing

This chapter presents the new architecture of biological signal measurement system and the new signal conditioner. This chapter concludes comparing result of the new signal conditioner and conventional one and characteristic of the proposed signal conditioner.

2.1 Biological Singal Processing

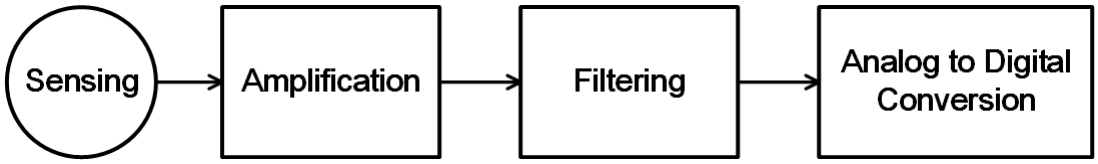


Figure 2.1: Biological Signal Processing

The architecture of biological signal processing is shown in Fig. 2.1. The biological signal from the sensing block has small amplitude and low frequency, the amplification block amplifies the amplitude of biological signal after sensing. The amplification block is required some characteristics as follows; the gain is variable, noise of this block is low. After amplification, the filtering block eliminates the signal such as the noise to acquire

the signal to noise ratio (SNR) for analog to digital conversion. The analog to digital conversion block convert analog signal to digital data.

2.2 Conventional Measurement System

Figure 2.2 shows example of the stationary type measurement system. The stationary type measurement system consists of analog front end (AFE), and PC. In addition, AFE and PC are connected by USB, therefore, this system is one of the wired system. AFE consists of an amplifier, a filter and an A/D converter. The stationary type measurement system is often used for medical, and this system has some advantages; this system has high accuracy and multi input channels and can be monitored measured data on real time. On the other hands, this system has an disadvantage of low portability. In many cases, The power supply of the stationary type measurement system is provided from PC.

Figure 2.3 shows example of the wearable type measurement system. The wearable type measurement system consists of AFE, PC (or smartphone), memory, communicator and battery. And this system is one of the wireless measurement system. The advantage of the wearable type measurement system is high portability, however, it requires many function and high cost.

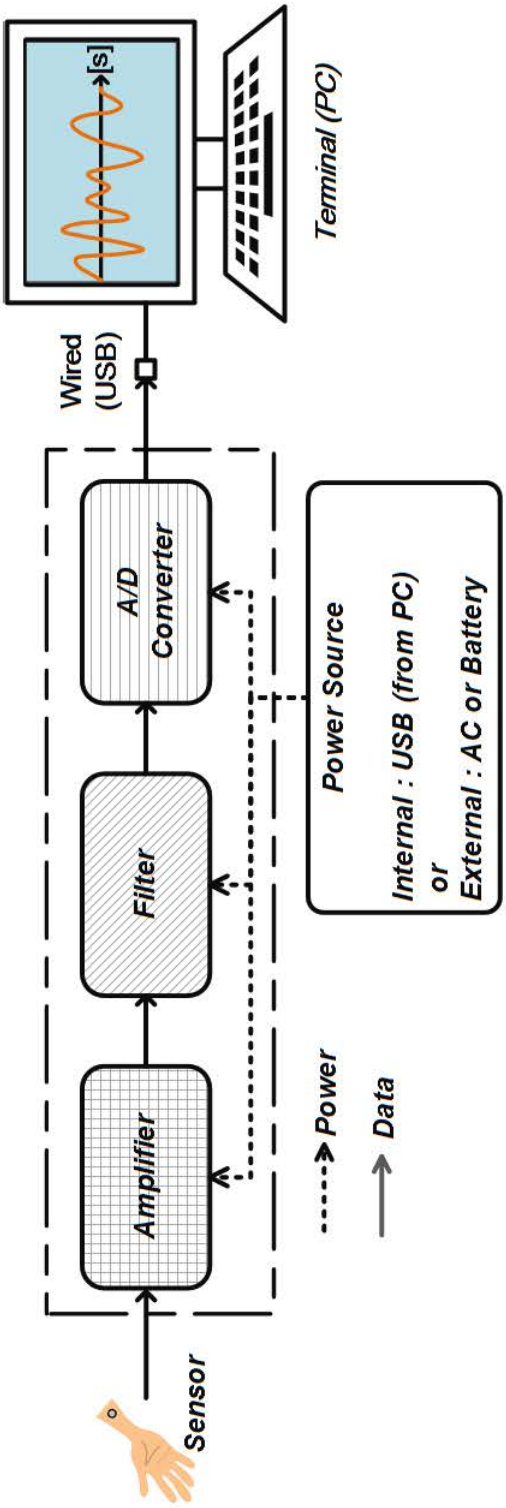


Figure 2.2: Stationary Type Measurement System

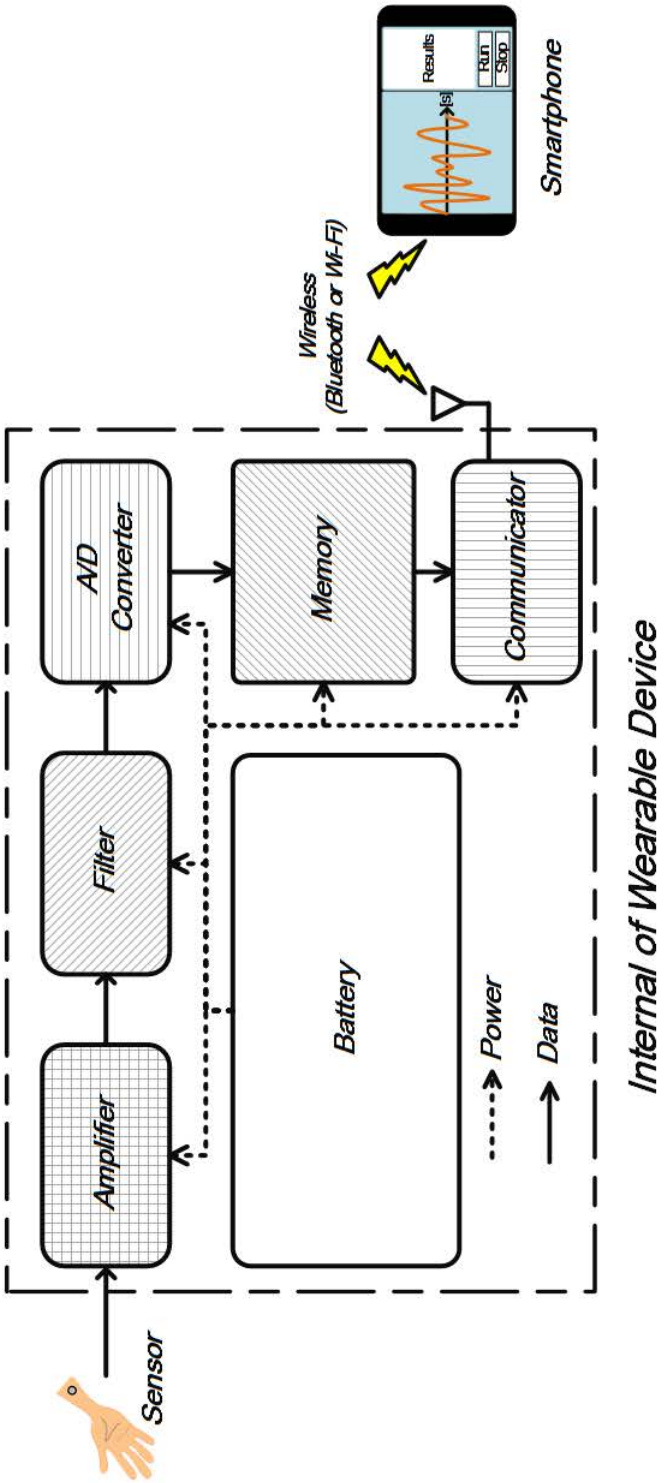


Figure 2.3: Wearable Type Measurement System

2.3 Proposed Measurement System

2.3.1 System Architecture

Figure 2.4 is proposed measurement system [29]. The proposed system consists of three circuit blocks; the instrumentation amplifier (IA), the filter and the voltage rectifier circuit. The IA is amplified input signal from sensor because the amplitude of biological signals very small. In this system, we adopted the IA, which has very high input impedance and CMRR. Furthermore, gain of the IA can be choose by the selecting a resistor. The low pass filter (LPF) is adopted in this system for eliminating the noise other than the target signal. Because the frequency of the biological signal is relatively low in general, the cut-off frequency of the LPF is less than 1000 Hz in this system. The voltage rectifier circuit of the last block is used for generating the DC power supplies. The audio signals, which are the sinusoidal waves, are generated by the application program in the smartphone, and the generated audio signals are outputted through earphone terminal of the smartphone. And then, these audio (sinusoidal) signals are converted to DC by the voltage rectifier circuit. This DC signals are used for the power sources for operating the circuits in the proposed system.

Comparing the conventional stationary type measurement system shown in Fig. 2.2, the proposed system can remove the A/D converter because the smartphone can receive analog signal directly through the microphone terminal, and the A/D converter is implemented in the smartphone. In addition, comparing the conventional wearable type measurement system, the proposed system can remove the A/D converter, the communicator and the battery.

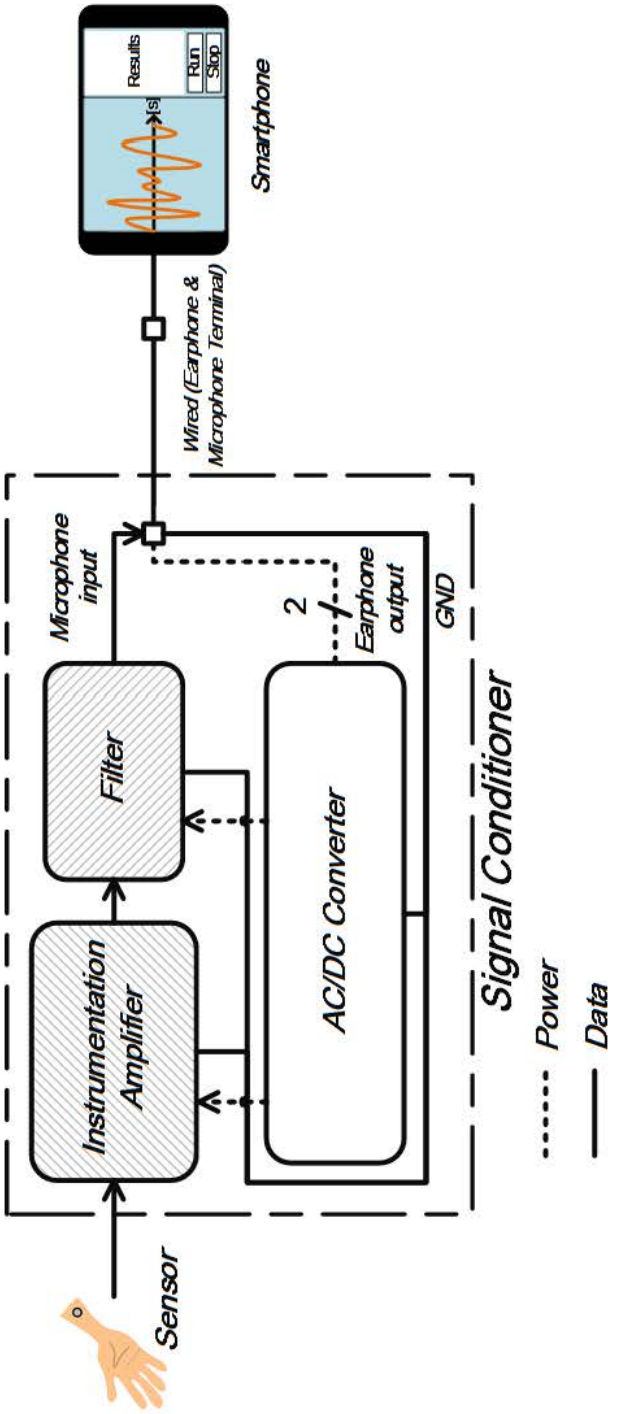


Figure 2.4: Proposed Measurement System

2.3.2 System Realization

Figure 2.5 shows the system realization using discrete parts.

R_G is resistor for selecting the gain of IA which is given by equation 2.1. In equation 2.1, α is constant value which depends on the device (decided by register network in IA), and selecting small R_G can be obtained high gain if we need.

$$gain = 1 + \frac{\alpha}{R_G} \tag{2.1}$$

R_{F1} and C_{F1} constitute of the LPF, and this LPF is necessary for reducing the noise in this system. The main noise in this system is the ripple which is occurred from voltage rectifier circuit, and the frequency of this noise is more than a few kHz. In the actual realization, we adopted a first order LPF with the cut-off frequency is approximately 600Hz.

voltage rectifier circuit shown in Fig. 2.5 is the sinusoidal wave to DC converter with voltage doubler, which outputs both positive and negative voltages. In the biological signal measurement system, analog circuit blocks need positive and negative voltage sources because the bias voltages is not added to the input signal from sensor. Furthermore, the output voltage from the earphone terminal is not generally so high, therefore we employed the voltage rectifier circuit with voltage doubler in order to operate all circuit blocks.

D_1 and C_2 constitute the well-known half-wave rectifier circuit. The voltage rectifier circuit with voltage doubler can be realized by adding to D_2 and C_1. By adding D_2 and C_1, the negative half cycle of the input signal from the earphone terminal charge C_1 and the next positive half cycle charge C_2 with adding the voltage of C_1. As the results, the positive voltage doubler can be achieved. In the same way, the circuit of the bottom side in voltage rectifier circuit shown in Fig. 2.5 also operates as the negative voltage doubler because the circuit has complementary structure of upper side one.

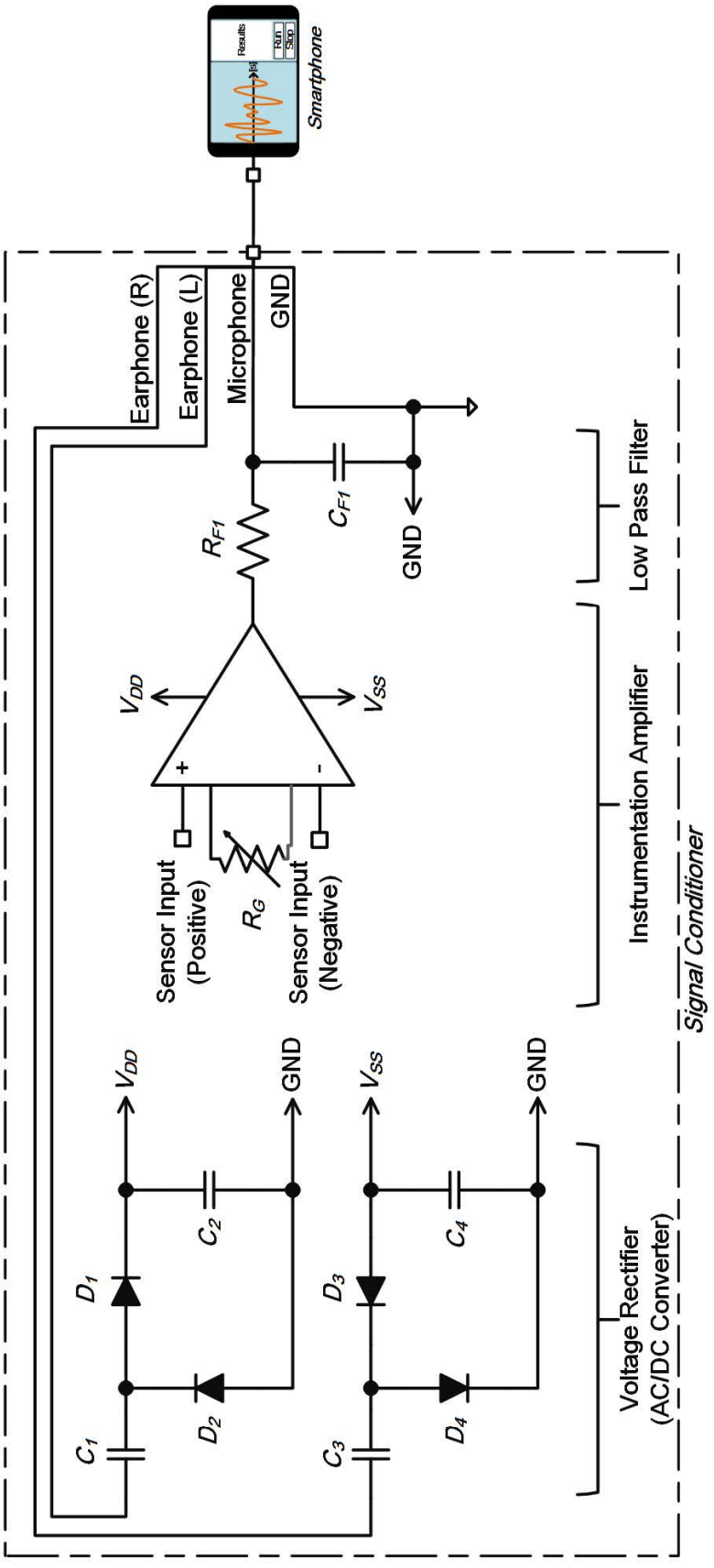


Figure 2.5: System Realization

Figure 2.6 shows activity diagram of proposed system [30][31][32]. This system has to execute input and output at the same time. In addition, input program and output program always have to work continuously. Therefore, that is realized using multi-thread programming. And, some button is required for user interface(UI).

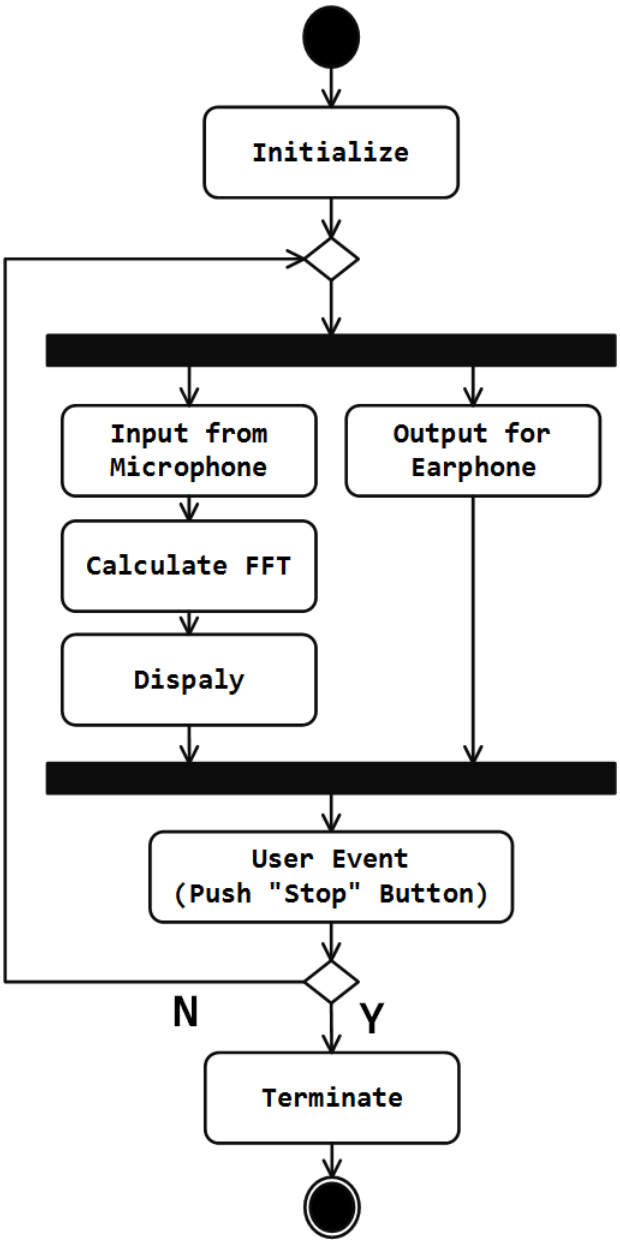


Figure 2.6: Activity Diagram of Proposed System

2.4 Experimental and Comparison Results

Figure 2.7 and Table 2.1 show photograph of overall of the proposed system and experimental condition, respectively. From Figure 2.7, it is clear that smartphone and the signal conditioner are connected only one wire. Gain of IA and cut-off frequency of LPF are configured 51 times and 605 Hz, respectively. And, the output signals of the earphone terminal consists of the amplitude of 1.5 V with the frequency of 10 kHz.

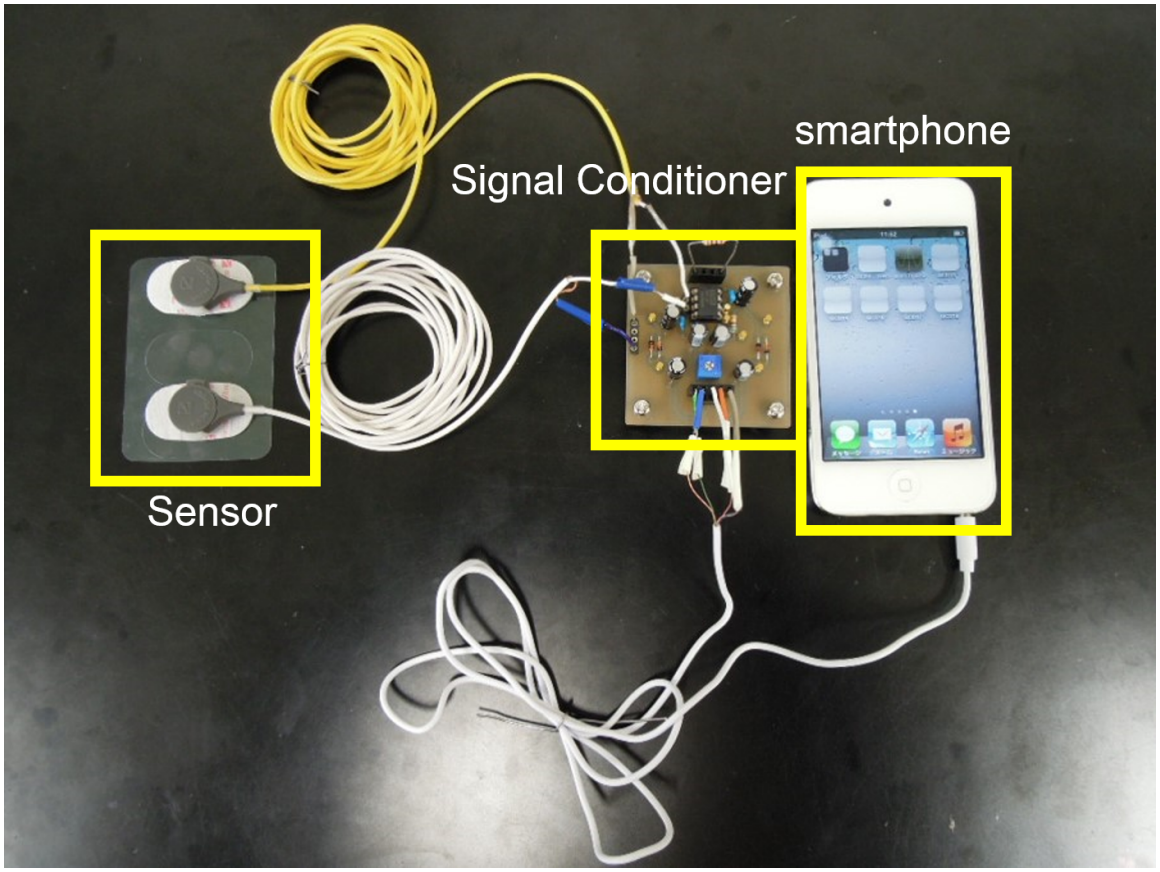
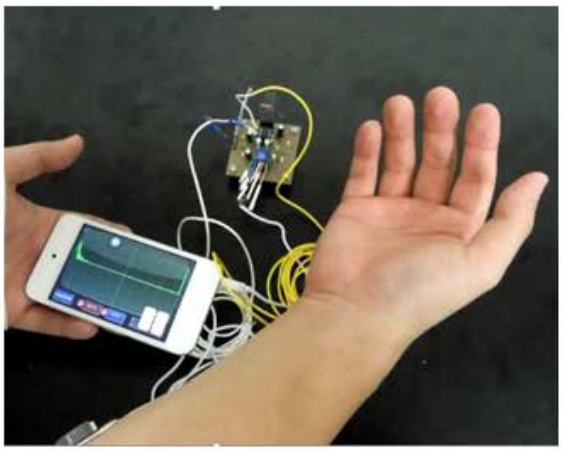


Figure 2.7: Photograph of Overall of the Proposed System

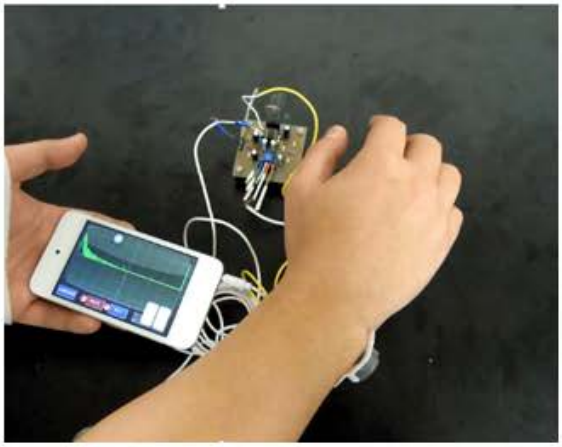
Table 2.1: Experiment condition

Item	Value
Smartphone	ipod touch 4th Gen.
Instrumentation Amplifier	INA118 [33]
D_1 – D_4	1N4148 [34]
C_1 – C_4	4.7 μF
R_G	1 kΩ
R_{F1}	560 Ω
C_{F1}	0.47 μF

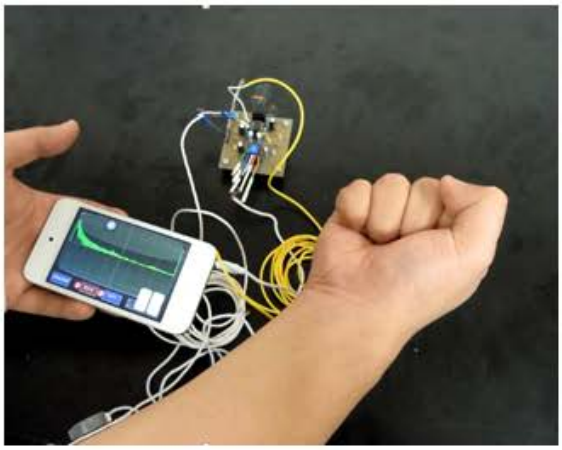
In this experiments, we employed the s-EMG signal as the biological signal. Figure 2.8 and Table 2.2 show results of s-EMG measurement. In Fig. 2.8, waveform, which are viewed on the display of the smartphone, shows results of the FFT analysis for the measured s-EMG signal. From Fig. 2.8, we can confirm that the waveforms in the case of neutral, pronation and grip are different. Furthermore, we could confirm that FFT results were changed according as moving the arm.



(a) Neutral



(b) Pronation



(c) Grip

Figure 2.8: Experimental Results

And, Table 2.2 shows experimental result for each subjects, and it is indicated that the proposed system could use generally. From these experimental results, the proposed system can be operated correctly.

Table 2.2: Experimental Result for each Subjects

Subject	Right Arm	Left Arm
A	○	○
B	○	○
C	○	○
D	○	○
E	○	○

Table 2.3 shows comparison result between the proposed and conventional systems. From Table 2.3, the proposed system could realize battery-less and low costs. However, comparing the wearable type measurement system, portability is decreasing by using wired connection. And comparing the stationary type measurement system the number of channels is only one in this situation. However, this disadvantage will be able to overcome the signal multiplexing techniques, which were proposed in the past [35][36][37].

Table 2.3: Comparison Result

Item	Proposed	Stationary	Wearable
Connection type	wired	wired	wireless
Battery	not require	not require	require
Costs (Number of Item)	Low	High	High
Portability	Mid.	Low	High
Resolution	depends on smartphone	High	Mid.
Number of channels	1 *	multi	1

* The number of channels can expand by using the signal multiplexing techniques.

2.5 Summary

In this chapter, new architecture of biological signal measurement system and very simple and battery-less signal conditioner, which consists of IA, filter and voltage rectifier circuit, have been proposed. The proposed measurement system operated correctly through the experiment with implemented system using the discrete parts and the smartphone. Comparing the conventional systems, the proposed system has advantages which are battery-less and low costs. In summary, the proposed system can be achieved the advantages by using implemented functions of the smartphone positively.

Chapter 3

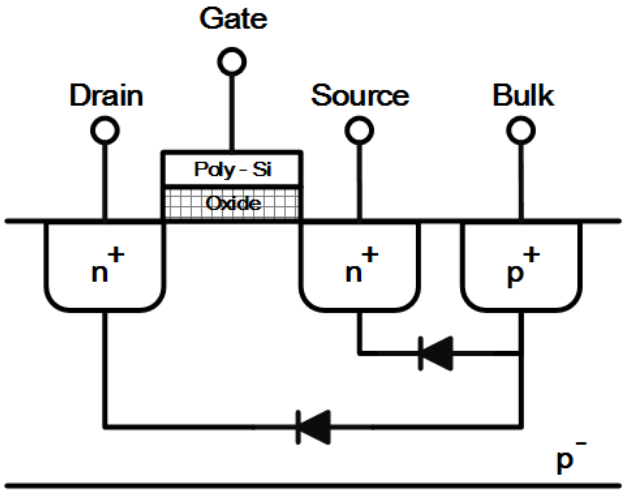
Integrated Voltage Rectifier Circuit

This chapter presents the new active diode with BRT and its application to voltage rectifier circuit. This chapter concludes experimental results; the new active diode with BRT eliminates the dead region, .

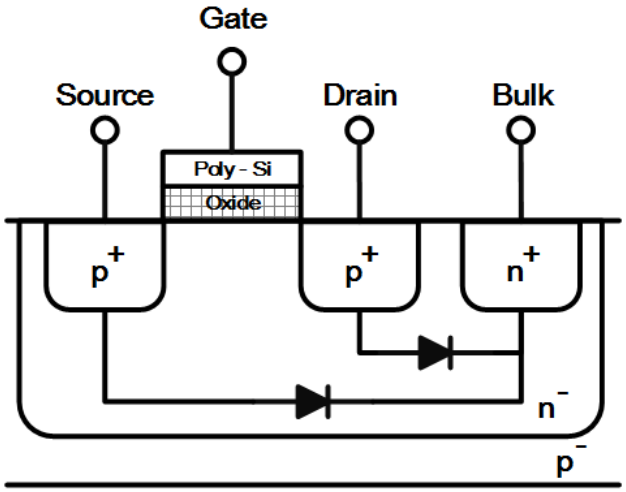
3.1 Integrated Diode

Figure 3.1: Symbol of Diode

Figure 3.1 shows the symbol of diode. The V_A and V_K are terminal voltages of the anode and the cathode. The operation of diode is as follows: In the case of $V_A > V_K$, the diode is turn on; In the case of $V_A < V_K$, the diode is turn off. Generally, the Si-diode has a potential barrier which is approximately 0.7 V. If the condition of $V_A > 0.7$, the current of diode increases exponentially. For this reason, the diode can rectify the AC signal.



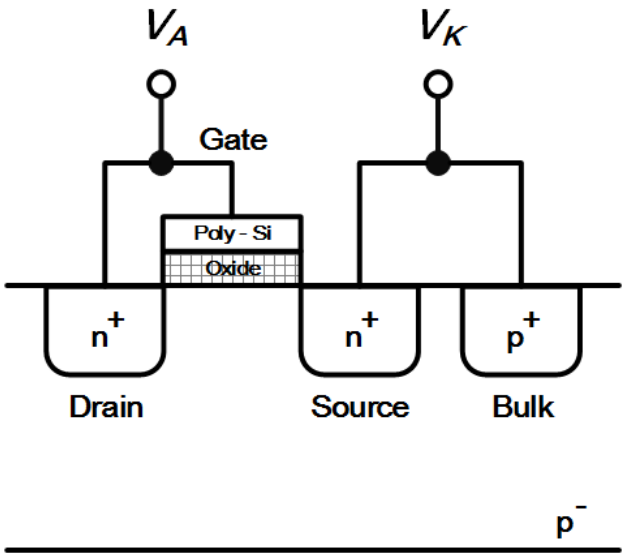
(a) NMOS Parasitic Diode



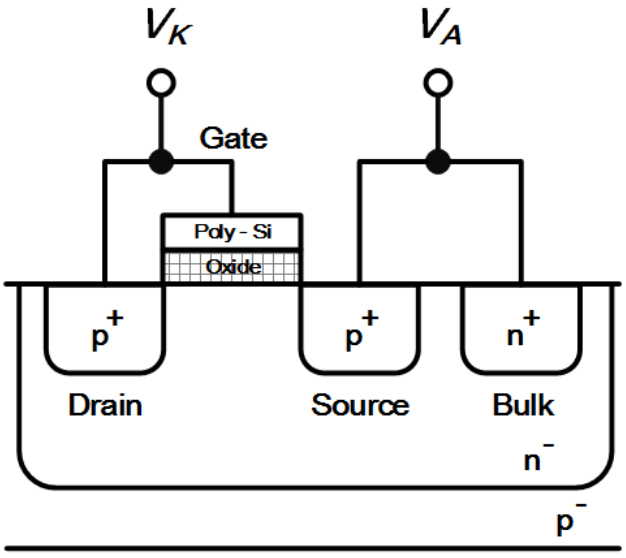
(b) PMOS Parasitic Diode

Figure 3.2: Parasitic Diodes of MOSFET

In the case of using the diode in the integrated circuit (IC), parasitic diode or MOS diode is used. Figure 3.2 shows the parasitic diodes of MOSFET which is example of standard CMOS process using n-well. The parasitic diodes of MOSFET are usually used parasitic diodes which are created between drain or source and bulk. Generally, using parasitic diodes of MOSFET have a problem which is leak current through the bulk terminal. Therefore, voltage of bulk terminals are set to V_{SS} (case of N-MOSFET) or V_{DD} (case of N-MOSFET).



(a) NMOS Diode



(b) PMOS Diode

Figure 3.3: Integrated Diodes of MOSFET

The MOS diode shown in Fig. 3.3 is usually used in IC. The drain and gate terminal are connected that means MOS transistor are always operated in saturation region. The drain current of MOS diode is as follows.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.1}$$

μ is mobility of MOSFET, C_{ox} is capacitance of gate oxide, W is channel width, L is channel length, V_{GS} is voltage between gate and drain terminal and V_{TH} is threshold voltage of MOSFET. If $1 \gg \lambda V_{DS}$ the drain current is as follows.

$$I_D \approx \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{3.2}$$

This equation indicates the current of MOS diode is proportional square of V_A. However, V_{TH} is not small value, and these diodes cannot eliminate it.

On the other hands, these diodes have the problem, that is V_K (voltage of bulk terminal) fixed V_{SS} (case of N-MOSFET) or V_{DD} (case of N-MOSFET). It means that the design flexibility decrease in single-well standard CMOS process. Overcoming this problem, the bulk regulation transistor (BRT) have been proposed [18]-[20].

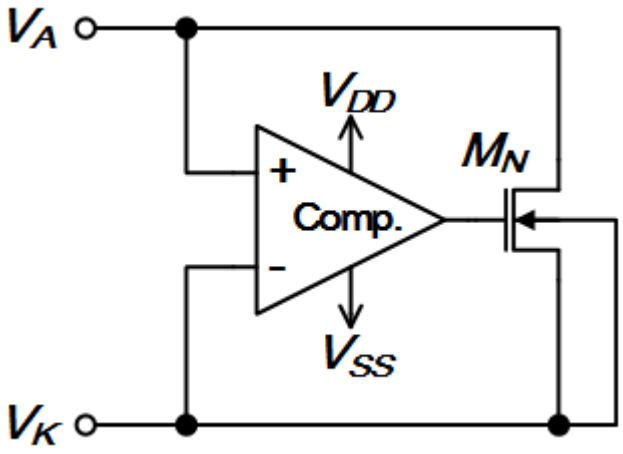
Figure 3.4 shows circuit schematic of each active diodes, that consist of a MOSFET and a comparator. The output of comparator connects gate terminal of MOSFET. The drain and source terminals are anode terminal V_A and cathode terminal V_K respectively. The comparator outputs comparing result of V_A and V_K. Operation of NMOS active diode shown in 3.4a is as follows: if $V_A > V_K$, comparator outputs High (V_{DD}) and MOSFET is turn on; if $V_A < V_K$, comparator outputs Low (V_{SS}) and MOSFET is turn off. Operation of PMOS active diode shown in 3.4b is complementary of NMOS active diode. The drain current of active diode is decided by voltage between drain and source terminal. In this situation, the drain current is as follows.

$$I_D = \mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2} \tag{3.3}$$

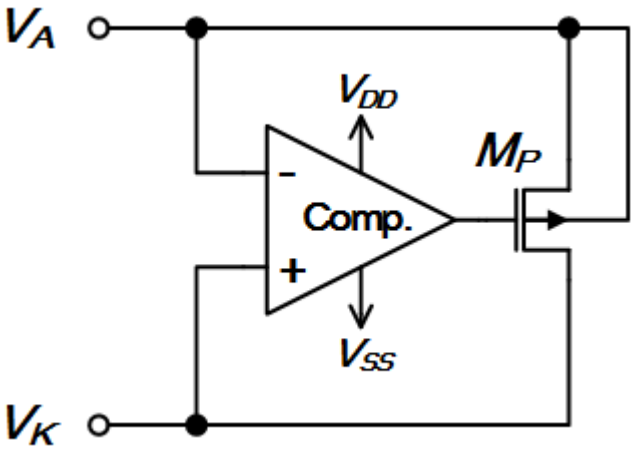
if $(V_{GS} - V_{TH})V_{DS} \gg \frac{{V_{DS}}^2}{2}$, the drain current is expressed as follows.

$$I_D \approx \mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{3.4}$$

if MOSFET is turn on, V_G is constant value, and V_K is connected to GND in generally.



(a) NMOS Active Diode



(b) PMOS Active Diode

Figure 3.4: Circuit Schematic of each Active Diodes

Therefore, the drain current is given by following equation.

$$I_D \approx \mu C_{ox} \frac{W}{L} (V_{DD} - V_{TH}) V_A \tag{3.5}$$

In this equation, $V_{DD} - V_{TH}$ is always constant value. For this reason, the drain current of active diode is proportional V_A. It means the drain current of active diode can be controlled by V_A and omitted V_{TH}. Figure 3.5 shows DC characteristic of each diodes, and it indicates that the active diode omit the threshold voltage.

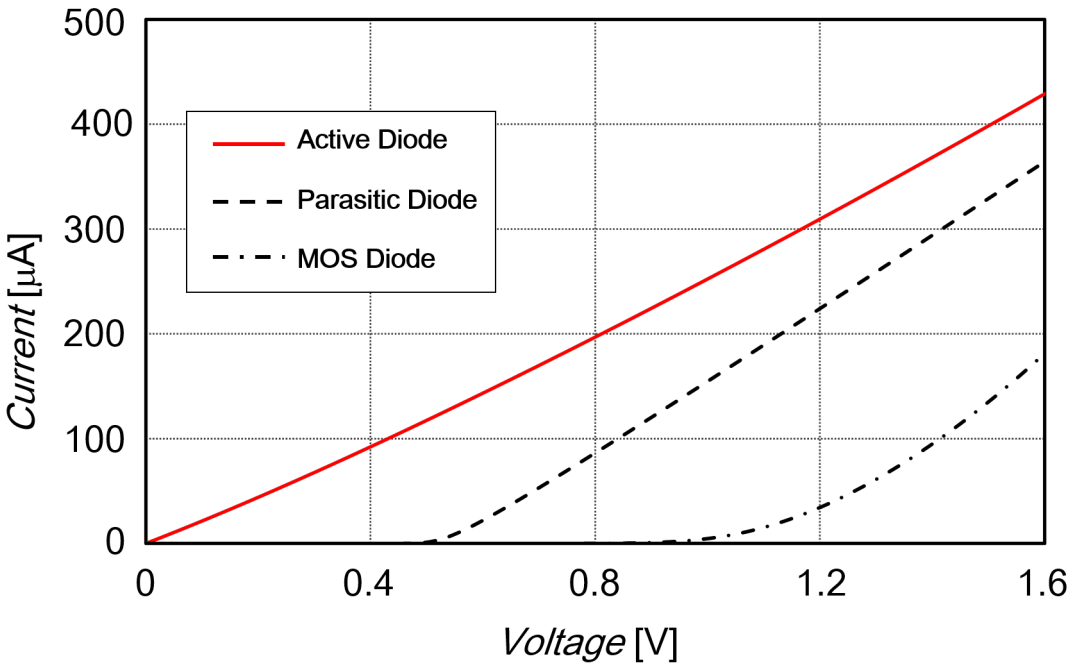


Figure 3.5: DC Characteristic of each Diodes

3.2 Conventional Active Diode with BRT

Figure 3.6 shows the circuit schematic of conventional active diode with BRT which is consisted of three MOSFETs and one comparator.

The operation of the active diode with BRT shown in Fig. 3.6 is different in the two voltage ranges that are $V_A > V_B$ and $V_A < V_B$, where V_A is terminal voltage of A and V_B is terminal voltage of B.

In the case of $V_A > V_B$, the terminals A and B are become the source and drain terminals respectively. As the results, the output of comparator becomes high, then M_1 turns off, and M_2 and M_3 turn on and off respectively. Therefore the terminal C is connected to terminal A (it is indicated the bulk of M_1 connect to own source terminal). In the case of $V_A < V_B$, the terminals A and B are become the drain and source terminals respectively. As the results, the output of comparator becomes low, then M_1 turns on, M_2 and M_3 turn off and on respectively. Therefore, the terminal C is connected to own source terminal.

From the above explanation, the terminal C, which is bulk terminal of M1, is always connected to own source terminal. In this way, the leak current through the bulk terminal (the parasitic diodes of M1) can be prevented. That is to say, the conventional active diode with BRT behaves like a diode with the threshold voltage of 0 V.

However, the conventional active diode with BRT shown in Fig. 3.6 has a problem in the switching operation of M_2 and M_3. Because V_{in} is AC signal (sinusoidal wave), M_2 and M_3 operate not only stable states of ON and OFF but also in the transitional region (dead region) which is not ON and OFF states. That is to say, the voltage of terminal C (V_C) is an indeterminate value in the dead region and the dead region is depend on the threshold voltage of MOSFET (V_T).

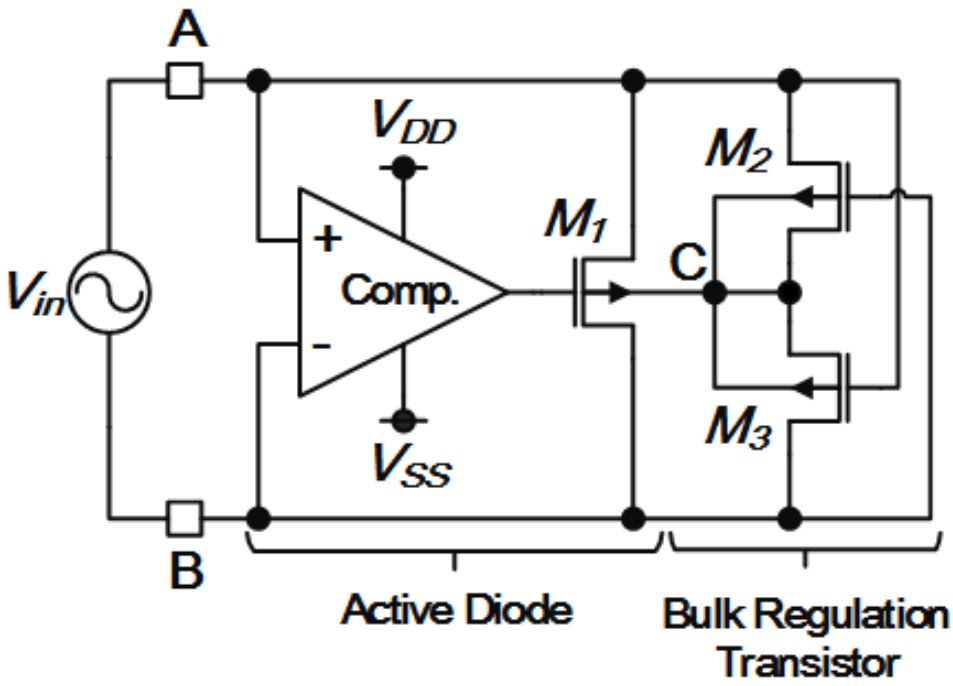


Figure 3.6: Conventional Active Diode with BRT

3.3 Proposed Active Diode with BRT

Figure 3.7 shows the circuit schematic of the proposed active diode with BRT. In order to overcome the dead region, the output of the comparator (V_{comp}) is used for the switching signal of M_2 and M_3 because V_{comp} does not output a voltage in the dead region but outputs the digital signal of High (V_{DD}) or Low (V_{SS}). In the actual design, an inverter is added for the switching control of M_2, as shown in Fig. 3.7.

The operation of the proposed active diode with BRT is almost same with conventional one. The differential of the operation of the proposed and conventional circuits is switching of BRT. V_{comp} is a digital signal, therefore the gate voltages of M_2 and M_3 are also digital signal. As the results, M_2 and M_3 turn ON or OFF in the moment. In this way, we can overcome the dead region problem [38].

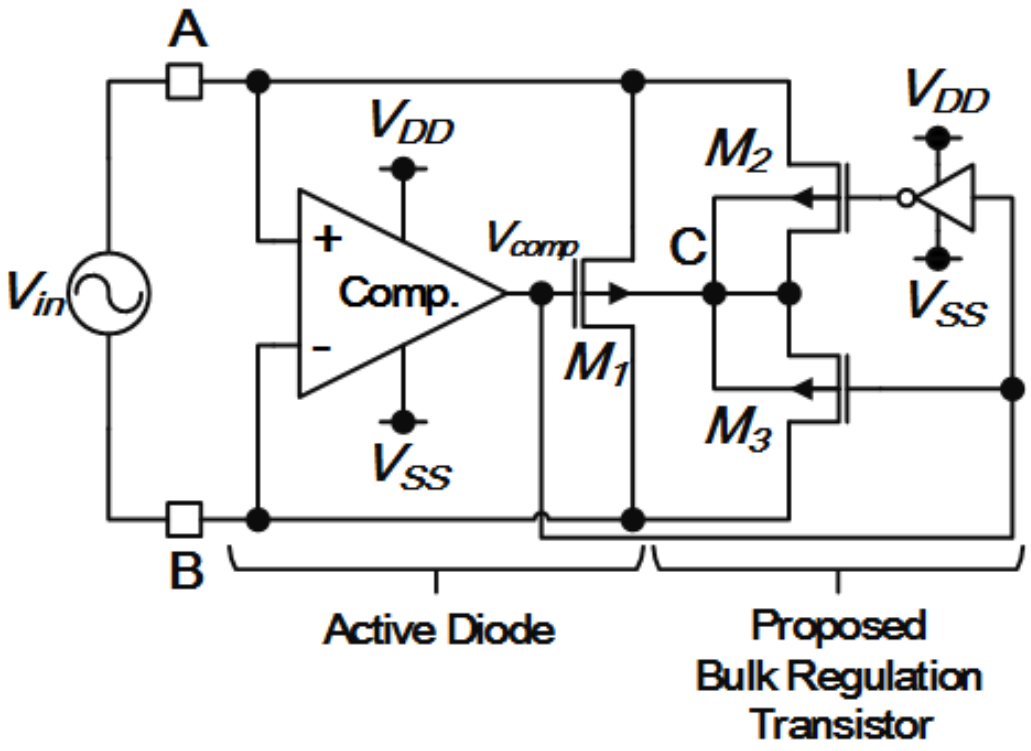


Figure 3.7: Proposed Active Diode with BRT

3.4 Application to Integrated Voltage Rectifier Circuit

Figure 3.8 shows the cisrcuit schematic of the conventional voltage rectifier circuit [21]-[28]. This circuit has two functions; one is conversion of the AC voltages to the DC voltages and the other is voltage doubler. Therefore, the output voltage of this circuit becomes the twice DC voltage of the amplitude of the input sinusoidal signal ideally. As shown in Fig. 3.8, the circuit consists of four diodes and four capacitors. This circuit operates as follows. D_1 and C_2 constitute the well-known half-wave voltage rectifier circuit. The voltage rectifier circuit with voltage doubler can be realized by adding to D_2 and C_1. By adding D_2 and C_1, in the negative half cycle of the input sinusoidal signal, C_1 is charged and in the next positive half cycle, C_2 is charged with adding the voltage of C_1. As the results, the positive voltage doubler can be achieved. In the same way, the circuit of the bottom side in the voltage rectifier circuit shown in Fig. 3.8 also operates as

the negative voltage doubler because the circuit has complementary structure of the upper side one. However, the output voltage of this circuit is decrease because the diodes has a threshold voltage. Furthermore, the problems of the stable operation and leak currents remain even if the conventional active diode with BRT is employed in stead of diode shown in Fig. 3.8.

Figure 3.9 shows the circuit schematic of the proposed voltage rectifier circuit. In the Fig. 3.9, the proposed active diode with BRT is employed in order to overcome the above problems. The voltage rectifier circuit is realized by replacing four diodes with the proposed active diode with BRT and the conventional active diode with BRT. Because the proposed circuit is designed by using single n-well process, the proposed active diode with BRT is applied to D_2 and D_3 and the conventional active diode is applied to D_1 and D_4. On the other hand, the proposed circuit can be divided to two circuit blocks as mentioned previously; positive and negative voltage doublers. Therefore, we can reduce the number of the comparators because the output signals of comparators can be shared since the circuit blocks of positive and negative voltage doublers have complementary structure each other. This contributes the reduction of the chip area and power consumption.

In the proposed circuit, two diodes can be replaced with the proposed active diodes with BRT, however, the remain two diodes cannot be replaced as mentioned previously. Therefore, the output voltage of the proposed rectifier circuit is slightly decrease compared with the ideal output. However, the output voltage of Fig. 3.9 is drastically improved as compared with that of Fig. 3.8 [38].

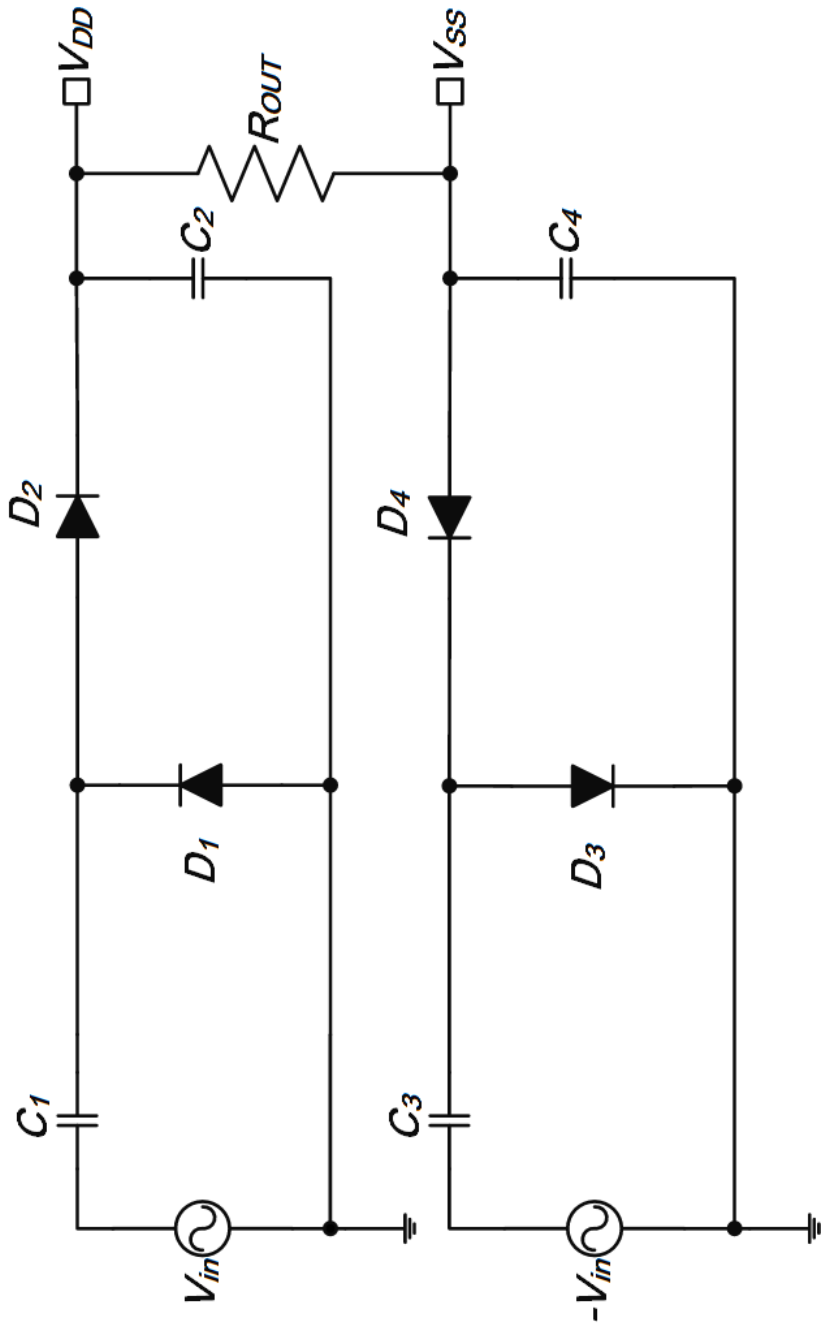


Figure 3.8: Conventional Voltage Rectifier Circuit

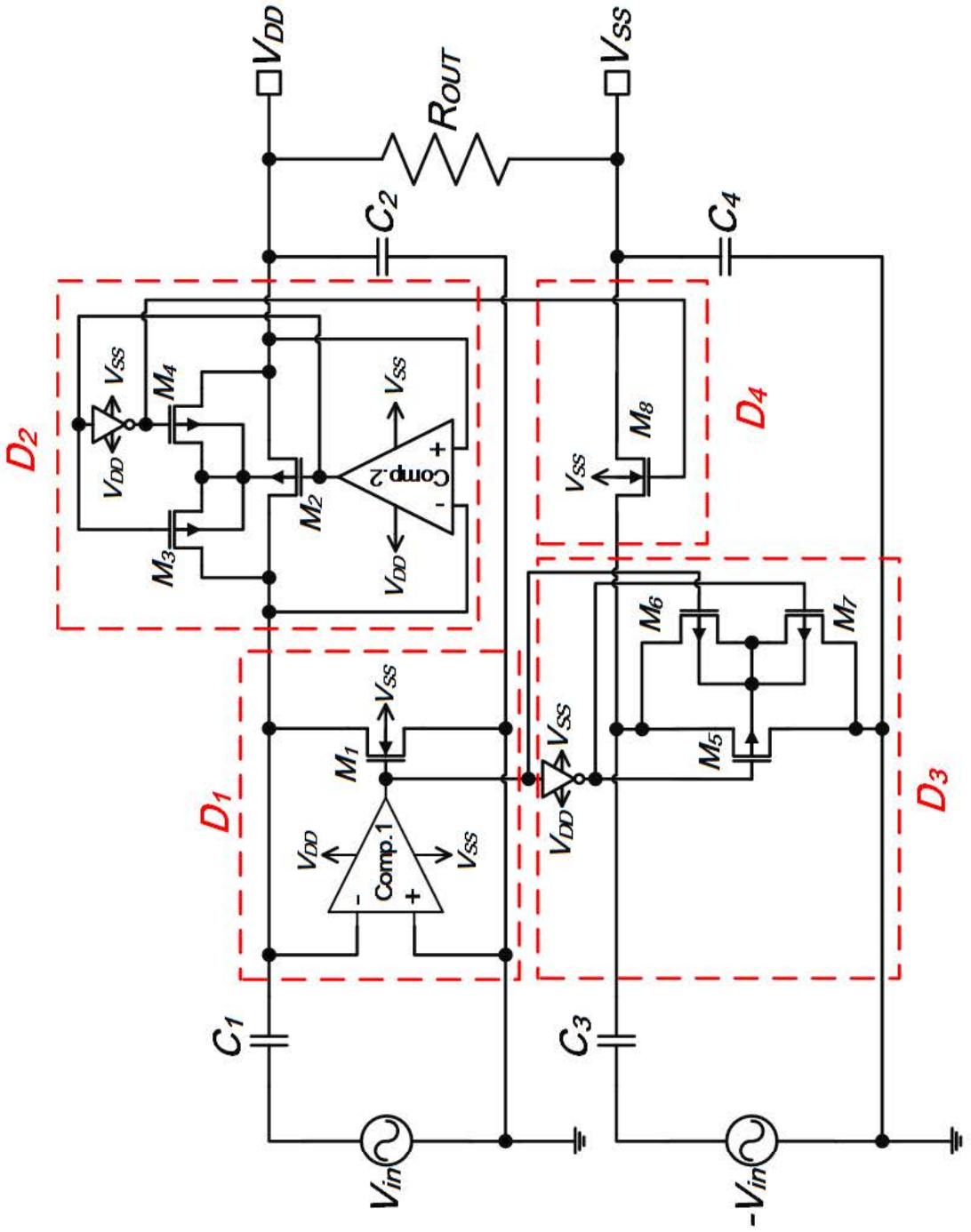


Figure 3.9: Proposed Voltage Rectifier Circuit

3.5 Simulation and Experimental Results

The proposed active diode with BRT shown in Fig. 3.7 and the proposed rectifier circuit shown in Fig. 3.9 were designed and fabricated by using 1-poly, 3-metal, single n-well, 0.6μm CMOS process. The design parameters are listed in Table 3.1.

Table 3.1: Design Value of each Devices

Item	Value
Channel Width (μm) / Channel Length (μm) of M_1, M_2, M_5, M_8	40 / 1 (10*)
Channel Width (μm) / Channel Length (μm) of M_3, M_4, M_6, M_7	10 / 1 (2*)
C_1 – C_4 (μF)	4.7
V_{DD}	2.5 V
V_{SS}	-2.5 V
Amplitude of V_{in}	1.5 V
Frequency of V_{in}	10 kHz

* This value means the number of parallel connection of MOSFET.

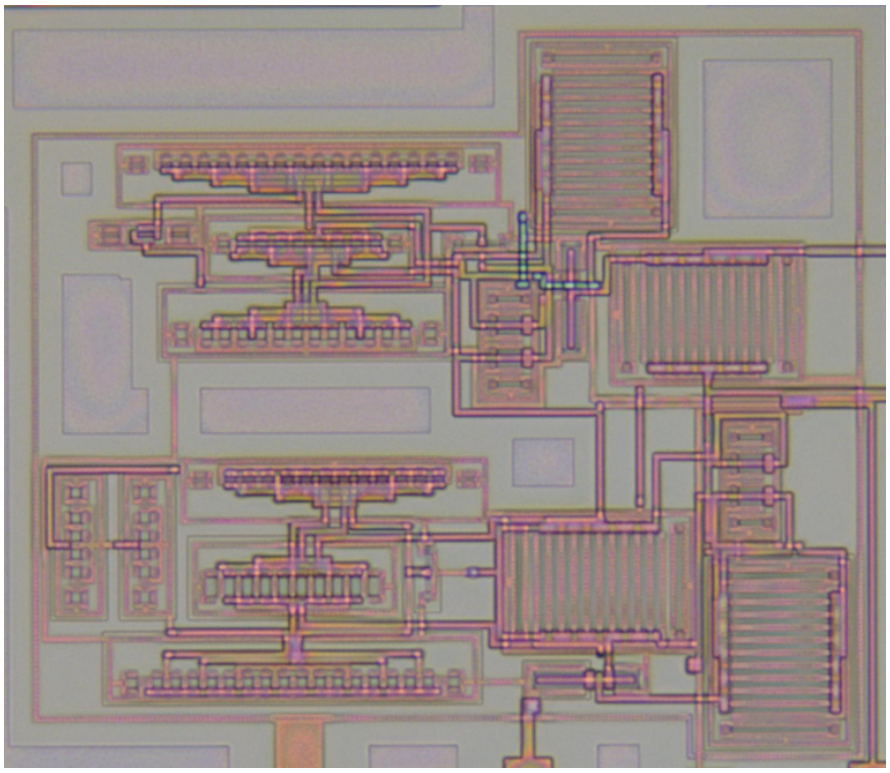


Figure 3.10: Photograph of the proposed voltage rectifier circuit

Figure 3.10 shows photograph of the proposed voltage rectifier. The area is 305 μm $\times$ 355 μm.

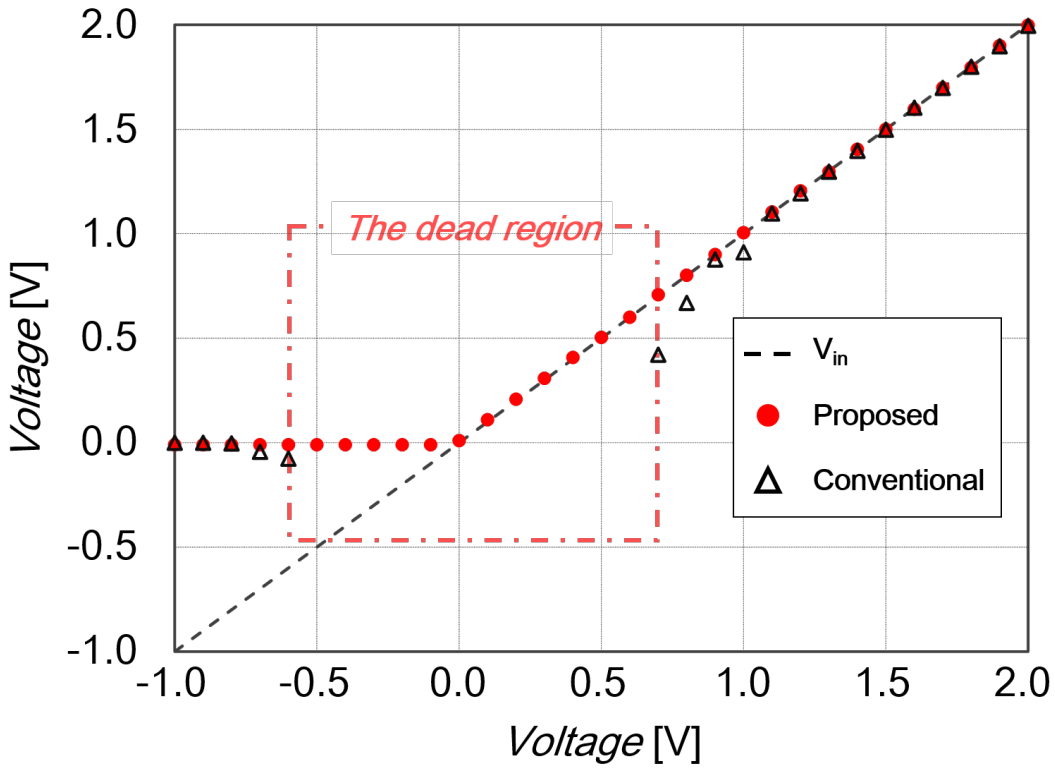


Figure 3.11: Relation between V_C and V_{in}

Firstly, we confirmed the I-V characteristics of the proposed and conventional active diodes shown in Fig. 3.6 and 3.7, respectively. As the results, we confirmed the threshold voltage of both circuits are the same and its value equals 0. Figure 3.11 shows the DC transfer characteristics of the the conventional and proposed active diode with BRT. In the Fig. 3.11, the vertical and horizontal axes mean V_C and the input voltage V_{in}, respectively. From this experimental results, the dead region exist in the conventional circuits and its range is from -0.6 V to 0.6V. In contrast the results, we can confirmed that the dead region is perfectly eliminated in the proposed one.

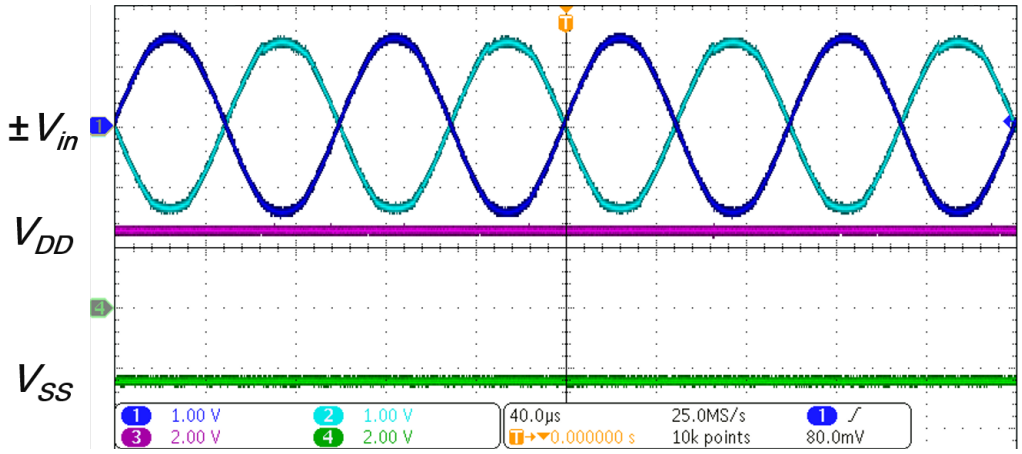


Figure 3.12: Oscilloscope photograph of the proposed voltage rectifier circuit

Figure 3.12 shows the oscilloscope photograph of the proposed voltage rectifier circuit. In this experiment, the amplitude and frequency of V_{in} were 1.5 V and 10 kHz, respectively, and $R_{OUT} = 10$ kΩ. From this graph, we can find the proposed voltage rectifier circuit generate the positive and negative power supply voltages, and its values are $+2.86$ V and -2.70 V.

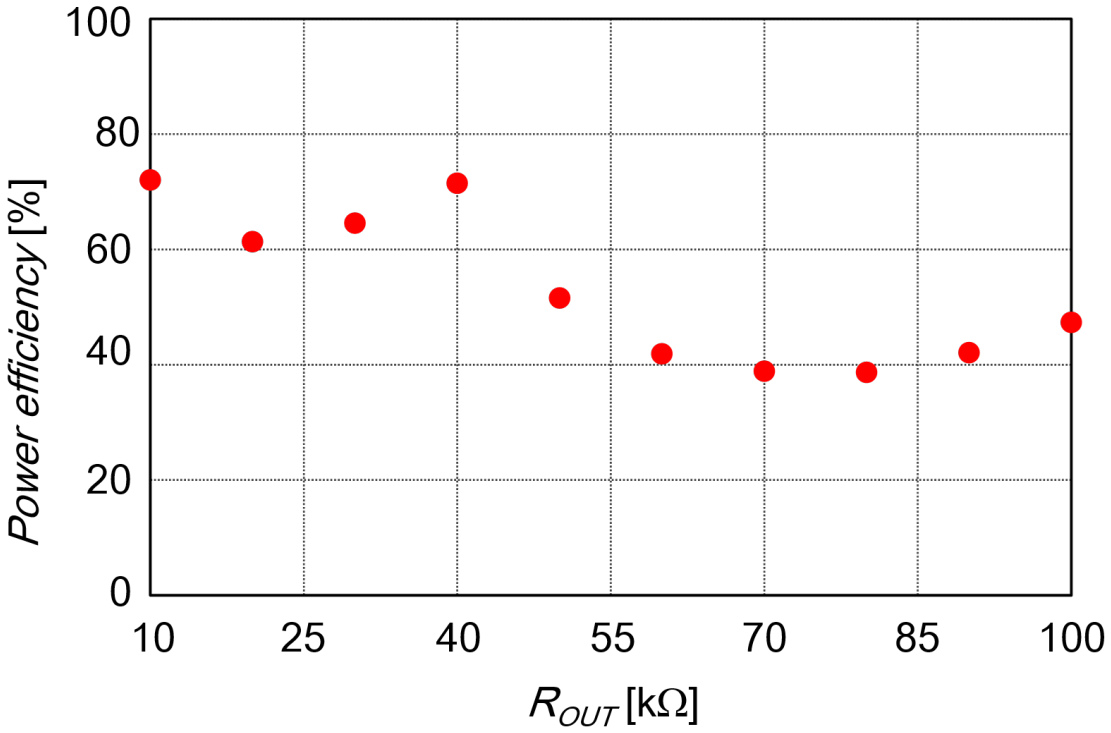


Figure 3.13: Experimental Result of Power Efficiency

Figure 3.13 shows power efficiency of the proposed voltage rectifier circuit. In this experiment, maximum power efficiency is 72.1 % @ $R_{out} = 10$ kΩ.

3.6 Summay

In this chapter, new active diode with BRT and its application to integrated voltage rectifier circuit have been proposed. We could confirmed that the proposed active diode with BRT can eliminate the dead region perfectly. Additionally, its application to integrated voltage rectifier circuit can reduce the chip area and the power consumption by sharing the output voltage of comparator, furthermore, the chip area, the output voltage and maximum power efficiency of the proposed voltage rectifier circuit are 305 μm $\times$ 355 μm and $+2.86$ V (positive side) and -2.70 V (negative side) and 72.1 %, respectively.

Chapter 4

Conclusion and Future Works

This thesis, simple architecture of biological measurement system and battery-less signal conditioner, which consists of IA, filter and voltage rectifier circuit, and the new active diode with BRT and its application to integrated voltage rectifier circuit have been proposed. Firstly, experimental and comparison results indicate that the proposed measurement system operated correctly through the experiment with implemented system using the discrete parts and the smartphone. Comparing the conventional systems, the proposed system has advantages which are battery-less and low costs. In summary, the proposed system can be achieved the advantages by using implemented functions of the smartphone positively. We could confirmed that the proposed active diode with BRT can eliminate the dead region perfectly. Additionally, its application to integrated voltage rectifier circuit can reduce the chip area and the power consumption by sharing the output voltage of comparator, furthermore, the chip area, the output voltage and maximum power efficiency of the proposed voltage rectifier circuit are 305 μm $\times$ 355 μm and $+2.86$ V (positive side) and -2.70 V (negative side) and 72.1 $\%$, respectively.

The future works are as follows; 1) implementing the integrated circuit of the signal conditioner by using references [39][40], 2) decreasing the power consumption by using references [41]–[45], 3) applying the startup method for the proposed voltage rectifier circuit. 4) expanding the number of channels, 5) comparing and evaluating the proposed system with marketed products, 6) designing the software of each operating system (Android, Windows mobile, etc.).

The proposed signal conditioner using the proposed integrated voltage rectifier circuit have already implemented. Figure 4.1 and Figure 4.2 show circuit schematic of all of proposed signal conditioner and photograph of the signal conditioner respectively. The IA is constructed by three operational amplifiers, which are two-stage operational amplifier using differential amplifier and common source amplifier [46]–[49]. Generally, register and capacitor, that construct LPF, require large chip area, therefore, the Gm-C filter is applied [50][51]. The filter, which is second order LPF, is constructed operational transconductance amplifier (OTA) and capacitors. From Fig. 4.2, chip area is 1.2 mm $\times$ 1.2 mm.

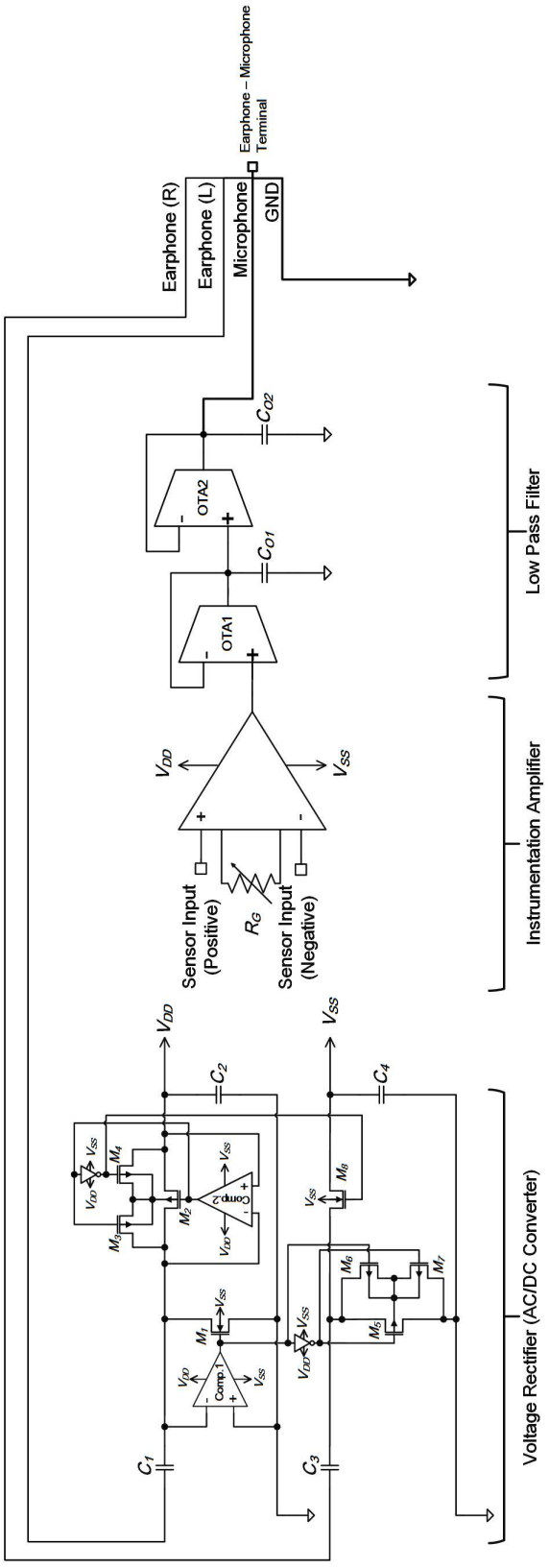


Figure 4.1: Circuit Schematic of Proposed Signal Conditioner

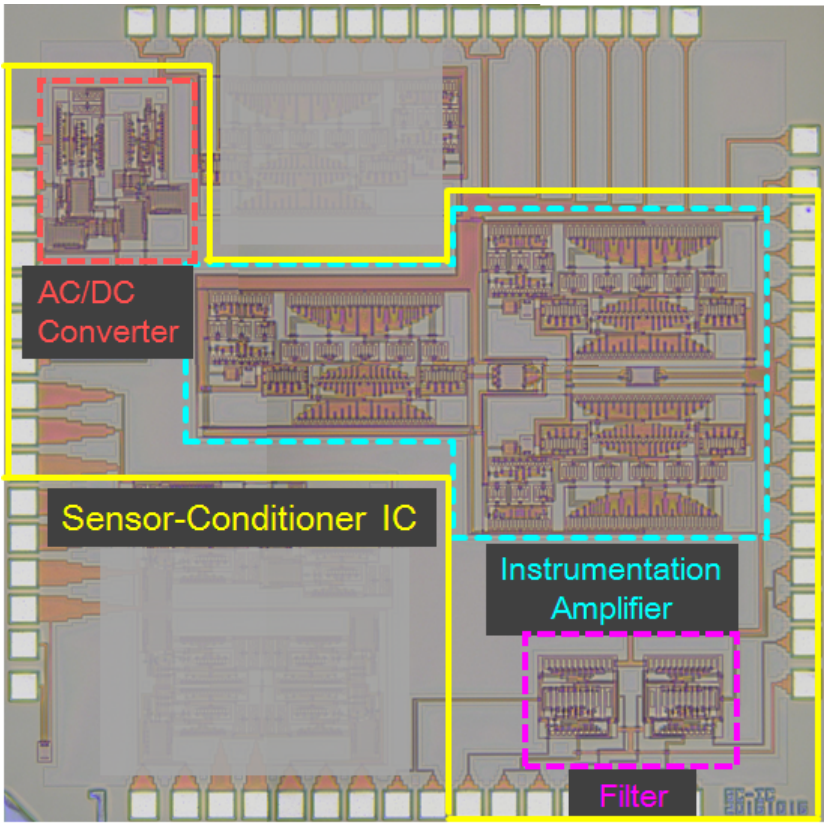


Figure 4.2: Photograph of the Implemented Signal Conditioner

Acknowledgments

The author would like to specially thank Prof. Koichi TANNO in University of Miyazaki, the author's principle adviser for indispensable suggestions and guidance during his researches in the doctor course of University of Miyazaki.

The author would like to thank Prof. Hiroki TAMURA, Masahiro TASUMI, and Hiroki MATSUMOTO for hopefull discussions and technical advises in various instructive fields.

The author is grateful to Mr. Agung Setiabudi, Mr. Yuto KAWASAKI, Masayuki UCHIHARA, Shigeru Taniguchi and Yuken Yakushiji for discussions and experiments.

The author is grateful to Ms. Takako TOYAMA, a technical staff in University of Miyazaki, for her technical support.

The author thanks to all laboratory members for their help, corporate and fun in laboratory life.

The author thanks to A.LSI Design Co., LTD., Toppan Technical Design Center Co., LTD., and Phenitec Semiconductor LTD., for their support of chip fablication.

The author thanks to VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc. and Mentor Graphics, Inc.

The author thanks to staff of interdisciplinary graduate school of agriculture and engineering in university of miyazaki for their help.

32 年間の生涯に渡り陰日向になりご支援いただいた父と母に深く感謝するとともに厚く御礼申し上げます．両親には，職を辞して学位を取得するという私の決断を最後まで支持いただいたこと，経済的，精神的に大きなご支援をいただいたことに感謝致します．また，兄と姉には，博士課程の期間に多くの激励の言葉をいただきました．このような家族に恵まれたことを誇りに思います．今後の研究者人生にて家族へ恩返しをしていきたいと思います．

最後に，私の人生の師である亡き祖父，祖母に本論文を捧げます．

References

[1] World Health Organization, ”World Health Statistics 2015,” WHO Press, 2015.

[2] United Nations, ”Population Division(2017),” *World Population Prospects: The 2017 Revision*, Working Paper No.ESA/P/WP/248.

[3] Ministry of Health, Labour and Welfare, ”Annual Health, Labour and Welfare Report 2013-2014 - For the Realization of a Society of Health and Longevity - ,” available from https://www.mhlw.go.jp/english/wp/wp-hw8/dl/summary.pdf, accessed on Dec. 3, 2018.

[4] Japanese Nursing Association, ”Nursing for the People with lifestyle-related diseases in Japan,” available from https://www.nurse.or.jp/jna/english/pdf/lifestyle-02.pdf, accessed on Dec. 12, 2018.

[5] D. Madhavi and B.V. Ramana, ”De-Identified Personal Health Care System Using Hadoop”, *IAES International Journal of Electrical and Computer Engineering*, vol. 5, no. 6, Dec. 2015

[6] T. Prayoga and J. Abraham, ”Behavioral Intention to Use IoT Health Device: The Role of Perceived Usefulness, Facilitated Appropriation, Big Five Personality Traits, and Cultural Value Orientations”, *IAES International Journal of Electrical and Computer Engineering*, vol. 6, no. 4, Aug. 2016

[7] J. W. Lee, H. K. Kim and H. K. Jung, "User Analysis Mechanisms based Mobile Fitness System", *IAES International Journal of Electrical and Computer Engineering*, vol. 6, no. 6, Dec. 2016

[8] G. Orecchini, L. Yang, M. M. Tentzeris and L. Roselli, "Wearable battery-free active paper printed RFID tag with human-energy scavenger", *IEEE MTT-S International Microwave Symposium*, pp. 1 - 4, June 2011.

[9] N. T. Dang, T. V. Tran and W. Y. Chung, "UHF wearable battery free sensor module for activity and falling detection", *Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 4812 - 4815, Aug. 2016

[10] T. Hilbel, S. Feilner, M. Struck and C. Hofmann, "Cor/log BAN BT a wearable battery powered mHealth data logger and telemetry unit for multiple vital sign monitoring", *Computing in Cardiology Conference*, pp. 273 - 276, Sept. 2016

[11] Q. Huang, Y. Mei, W. Wang and Q. Zhang, "Battery-free sensing platform for wearable devices: The synergy between two feet", *IEEE International Conference on Computer Communications*, pp. 1 - 9, April 2016.

[12] G. Z. Yang, B. M. G. Rosa, "A wearable and battery-less device for assessing skin hydration level under direct sunlight exposure with ultraviolet index calculation", *IEEE Wearable and Implantable Body Sensor Networks*, pp. 201 - 204, March 2018.

[13] A. Setiabudi, H. Tamura and K. Tanno, "CMOS Temperature Sensor with Programmable Temperature Range for Biomedical Applications", *IAES International Journal of Electrical and Computer Engineering*, vol. 8, no. 2, April 2018.

[14] A. Kazantsev, J. Ponomareva, P. Kazantsev, R. Digilov and P. Huang, "Development of e-health network for in-home pregnancy surveillance based on artificial intelligence", *Proc. of 2012 IEEE-EMBS International Conference on Biomedical and Health Informatics*, pp. 82-84, 2012.

[15] Z. Che and Y. Liu, "Deep Learning Solutions to Computational Phenotyping in Health Care", *2017 IEEE International Conference on Data Mining Workshops*, pp. 1100-1109, 2017.

[16] M. Makikawa, M. Yoshida, M. Nambu, N. Shiozawa and S. Okada, Measurement technologies of mind and body condition in daily life for the development of human friendly products, CORONA PUBLISHING CO., LTD, 2010.

[17] J. Rumbaugh, I. Jacobson and G. Booch, Biomedical Signal Processing and Signal Modeling, Wiley-Interscience, 2000.

[18] Y. Rao and D.P. Arnold, "An AC/DC Voltage Doubler with Configurable Power Supply Schemes for Vibrational Energy Harvesting", *IEEE Applied Power Electronics Conference and Exposition*, pp. 2844-2851, 2013.

[19] D. Maurath, et al., "Highly efficient integrated rectifier and voltage boosting circuits for energy harvesting applications," *Advances in Radio Science*, Vol.6, pp. 219-225, 2008.

[20] C. Peters, et al., "A Sub-500 mV Highly Efficient Active Rectifier for Energy Harvesting Applications," *IEEE Transactions on Circuits and Systems*, Vol. 58, No. 7, pp. 1542-1549, 2011.

[21] T. Lehmann, Y. Moghe, "On-Chip Active Power Rectifiers for Biomedical Applications," *IEEE International Symposium on Circuits and Systems*, Vol.1, pp. 524-527, 2005.

[22] E.Dallago, et al., "Active Autonomous AC-DC Converter for Piezoelectric Energy Scavenging Systems," *IEEE Custom Integrated Circuits Conference*, pp. 555-558, 2008.

[23] G. Gosset, D. Flandre, ”A very high efficiency ultra-low-power 13.56 MHz voltage rectifier in 150nm SOI CMOS,” *IEEE International Symposium on Radio-Frequency Integration Technology*, pp. 347-350, 2009.

[24] Y. Da and A. Khaligh, ”Hybrid offshore wind and tidal turbine energy harvesting system with independently controlled rectifiers,” *2009 35th Annual Conference of IEEE Industrial Electronics*, pp. 4577 - 4582, 2009.

[25] D. Karolak, T.Taris, Y. Deval, Jean-Baptiste Béguéret, A. Mariano, ”Design Comparison of Low-Power Rectifiers Dedicated to RF Energy Harvesting,” *IEEE International Conference on Electronics, Circuits, and Systems*, pp. 524-527, 2012.

[26] H. Rabén, J. Borg and J. Johansson, ”An active MOS diode with Vth-cancellation for RFID rectifiers,” *2012 IEEE International Conference on RFID*, pp. 54 - 57, 2012.

[27] H. Ulusan, K. Gharehbaghi, Ö. Zorlu, A. Muhtaroglu and H. Külah, ”A self-powered rectifier circuit for low-voltage energy harvesting applications,” *2012 International Conference on Energy Aware Computing*, pp. 1 - 5, 2012.

[28] X. D. Do, H. H. Nguyen, S. K. Han and S. G. Lee, ”A rectifier for piezoelectric energy harvesting system with series Synchronized Switch Harvesting Inductor,” *2013 IEEE Asian Solid-State Circuits Conference*, pp. 269 - 272, 2013.

[29] R. Miyauchi, K. Tanno and H. Tamura, ”Simple Measurement System for Biological Signal Using a Smartphone,” *IAES International Journal of Electrical and Computer Engineering*, vol. 8, no. 6, Dec. 2018.

[30] J. Vlissides, R. Johnson, R. Helm and E. Gamma, ”Design Patterns: Elements of Reusable Object-Oriented Software,” Addison-Wesley Professional, 1994.

[31] J. Rumbaugh, I. Jacobson and G. Booch, Unified Modeling Language Reference Manual, 2nd ed., Addison-Wesley Professional, 2004.

[32] T. Parveen, Textbook of Operational Transconductance Amplifier and Analog Integrated Circuits, I K International Publishing House, 2009.

[33] INA118, Precision, Low Power Instrumentation Amplifier, Texas Instruments Inc., Dallas, Sep. 2000[Online], available from http://www.ti.com/product/ina118, accessed on March 5, 2018.

[34] 1N4148, High Conductance Fast Diode, On Semiconductor Inc., Phoenix, June 2015[Online], available from http://www.onsemi.com/PowerSolutions/product.do?id=1N4148, accessed on March 5, 2018.

[35] Khosro Rajabpour-Moghaddam, Mohammad Maymandi-Nejad, H. K. Ghomash, "A 24-channel implantable neural recording based on time and frequency-division multiplexing", *Analog Integrated Circuits and Signal Processing*, Vol. 79, Issue 3, pp. 493-506, June, 2014.

[36] X. Zhao, V. Sadhu and D. Pompili, "Analog Signal Compression and Multiplexing Techniques for Healthcare Internet of Things", *IEEE International Conference on Mobile Ad Hoc and Sensor Systems*, pp. 398-406, 2017.

[37] K. Tanno, Y. Sugahara and H. Tamura, "High-linear four-quadrant multiplier based on MOS weak-inversion region translinear principle with adaptive bias technique," *2011 IEEE Region 10 Conference*, pp. 680 - 684, 2011.

[38] R. Miyauchi, K. Tanno and H. Tamura, "New Active Diode with Bulk Regulation Transistors and Its Application to Integrated Voltage Rectifier Circuit," *IAES International Journal of Electrical and Computer Engineering*, vol. 9, no. 2, April 2019.

[39] Z. Abidin, K. Tanno, S. Mago and H. Tamura, "Low Common-Mode Gain Instrumentation Amplifier Architecture Insensitive to Resistor Mismatches", *IAES International Journal of Electrical and Computer Engineering*, vol.6, no. 6, Dec. 2016.

[40] Z. Abidin, K. Tanno, S. Mago and H. Tamura, "A New Instrumentation Amplifier Architecture Based on Differential Difference Amplifier for Biological Signal Processing", *IAES International Journal of Electrical and Computer Engineering*, vol.7, no. 2, April 2017.

[41] B. P. Sharma and R. Mehra, "Design of CMOS instrumentation amplifier with improved gain & CMRR for low power sensor applications," *2016 2nd International Conference on Next Generation Computing Technologies*, pp. 72 - 77, 2016.

[42] A. Jain and K. Kandpal, "Design of a high gain, Temperature Compensated Biomedical Instrumentation Amplifier for EEG Applications," *2016 2nd International Conference on Next Generation Computing Technologies*, pp. 292 - 296, 2017.

[43] T. A. Vu, et al., "Low-Power D-Band CMOS Amplifier for Ultrahigh-Speed Wireless Communications", *IAES International Journal of Electrical and Computer Engineering*, vol. 8, no. 2, April 2018.

[44] O. T. Weng, et al., "Low Power CMOS Electrocardiogram Amplifier Design for Wearable Cardiac Screening", *IAES International Journal of Electrical and Computer Engineering*, vol. 8, no. 3, June 2018.

[45] M. Kaur, J. Kaur, "IDDQ Testing of Low Voltage CMOS Operational Transconductance Amplifier", *IAES International Journal of Electrical and Computer Engineering*, vol. 8, no. 3, June 2018.

[46] R. L. Geiger, P. E. Allen and N. R. Strader., "VLSI Design Techniques for Analog and Digital Circuits," McGraw-Hill, 1990.

[47] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2000.

[48] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," Wiley, 2001.

[49] R. J. Baker, ”CMOS Circuit Design, Layout, and Simulation,” McGraw-Hill, 2001.

[50] C. Toumazou, F. J. Lidgey and D. G. Haigh, Analogue Ic Design: The Current-Mode Approach, Peter Peregrinus Ltd, 1990.

[51] K. Tanno, H. Tanaka, R. Miwa and H. Tamura, ”Wide-common-mode-range and high-CMRR CMOS OTA operable in both weak and strong inversion regions,” *2008 IEEE Asia Pacific Conference on Circuits and Systems*, pp. 1180 - 1183, 2011.