Expandable MVL CMOS Inverter and Its Application to MVL CMOS Hysteresis Comparator without Backgate Scheme

Arif Abdul MANNAN[a], Hiroki TAMURA[b], Takako TOYAMA[c], Koichi TANNO[d]

Abstract

In this paper, a novel voltage-mode MVL inverter is proposed. The proposed inverter consists of two circuit blocks: MVL threshold comparator and Multi-level generator, which can be implemented by standard CMOS technologies. Next, the inverted MVL hysteresis comparator is also proposed as the application of the proposed MVL inverter. The proposed MVL inverter and inverted MVL hysteresis comparator are expandable, capable to use more numbers of levels in MVL circuits. The performances of all proposed MVL circuits were evaluated through HSPICE with the set of 0.18μm CMOS process parameters. From the simulation results, we could confirm that all proposed MVL circuits work well as theory.

Keywords: Multiple-Valued Logic; Inverter; Threshold Detector; Hysteresis Comparator

1. INTRODUCTION

Recently, Multiple-Valued Logic (MVL) has been attracting many researchers and engineers because MVL is one of the possible solutions to problem of increasing complexity, interconnection and power consumption of the binary systems, especially at ultra large-scale integration (ULSI).

Needless to say, inverter is one of the most important circuit elements for implementing the digital circuits; of course, MVL inverter is also important circuit element for the MVL circuits. In the past, some MVL inverters used in the voltage-mode have been proposed [1]-[7].

The first approach is to use RTD devices, or bipolar transistor, or depletion MOSFETs, which has advantage of very high speed [1],[2],[6]. However, the fabrication cost is high because it is not compatible with standard CMOS process. The second approach is to use floating gate or semi-floating gate MOSFETs, which is simple circuit configuration [3]-[5]. However, this kind of device requires many capacitances, therefore large area is occupied in a chip. The third approach is to use the ordinary MOSFETs, which is very simple and compatible with standard CMOS process. Therefore the fabrication cost is low [7]. However, this circuit requires the multiple supplies such as 0.6V, 1.2 V and 1.8V in the case of four-valued logic.

In this paper, we proposed new multiple-valued logic circuits; MVL inverter and MVL hysteresis comparator. The proposed circuits are compatible with standard CMOS process and can be operated at only one supply. Furthermore, the core circuit used in the proposed circuits, which are the MVL threshold detector and Multi-level generator, can be expanded to many valued logics easily. The MVL threshold detector, feedback scheme and back gate scheme are also combined to create MVL hysteresis comparator. The simulation results, evaluation, and limitation of the proposed circuits are shown in this paper.

2. EXPANDABLE MVL INVERTER

For expandable MVL inverter circuit, the number of "n"-valued logic is representation of the number of level on MVL inverter. Consider an n-valued inverter, has n number of values, consists of Vi, which i = {0, 1, 2, …,n-1}.

The proposed MVL inverter circuit is consists of two core circuits, MVL threshold detector and Multi-level generator. Each core circuits of the MVL inverter are designed as inverted circuit, simplify the overall design and can be expanded to many more logic values easily. The proposed MVL inverter block diagram is shown in Fig. 1. Each block is explained below.

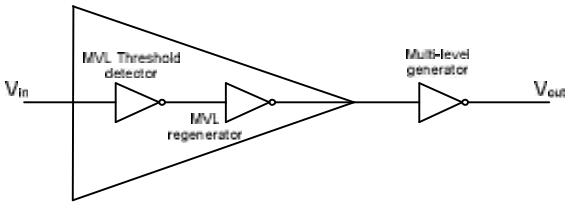

Figure 1. Block diagram of proposed MVL inverter circuit

a) Master Student, Graduate School of Engineering
b) Associate Professor, Dept. of Electronic and Electrical Engineering
c) Technical Staff, Dept. of Electronic and Electrical Engineering
d) Professor, Dept. of Electronic and Electrical Engineering

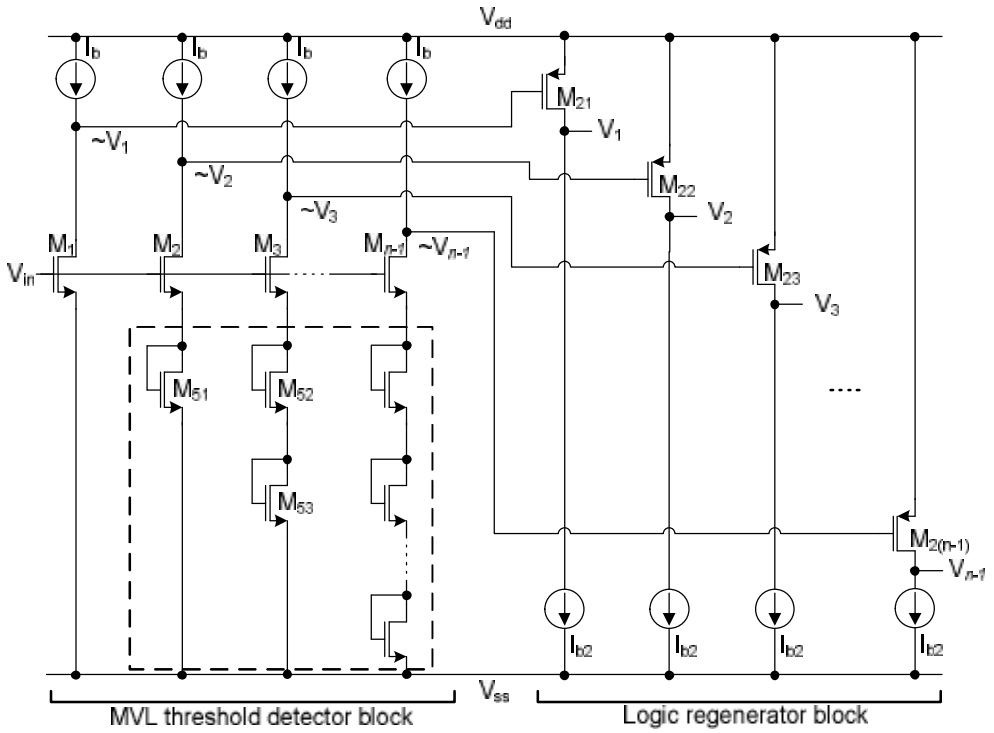

Figure 2. Circuit schematic of the proposed expandable MVL threshold detector (MVL threshold detector block and logic regenerator block)

A. EXPANDABLE MVL THRESHOLD DETECTOR

Fig. 2 shows the proposed MVL threshold detector. The MVL threshold detector is designed to generate n-1 level of threshold voltage. The proposed MVL threshold detector is divided into two blocks: MVL threshold detector block and logic generator block (see Fig. 2).The MVL regenerator is a circuit to regenerate the output voltage of MVL threshold detector, cause the $\sim V_i$ output has V_{dd} and V_{ss} level. Since MVL regenerator is also inverted, the output of the circuit is V_i through the logic generator block. Firstly, the operation of the MVL threshold detector block is explained.

In Fig.2, each NMOSFET M_1, M_2, M_3, and M_{n-1} operates as a switch. All MOSFETs inside dotted line operate as V_{gs} generator. If MOS switches turn on, the I_b flow through MOSFETs of V_{gs} generator. The MOSFETs are operated in the saturation region since gate is connected to own drain. Therefore, V_{gs} of the V_{gs} generator can be given by

$$V_{gs} = \sqrt{\frac{I_{ds}}{K_0} \cdot \frac{L}{W}} + V_T \tag{1}$$

where K_0 is unit transconductance parameter, W and L are channel width and length, respectively, I_{ds} is drain-to-source current, and V_T is threshold voltage. If we set I_b is enough small value, from (1), we can obtain

$$V_{gs} \approx V_T \tag{2}$$

From (2), each MOSFET inside the dotted line generates V_T. If the threshold voltages of all MOSFETs inside the dotted line are the same value, the output voltage of the MVL threshold detector block can be given by

$$\sim V_i \approx \begin{cases} V_{dd} & V_{in} < i \cdot V_T \\ (i-1)V_T & V_{in} \geq i \cdot V_T \end{cases} \tag{3}$$

where i is 1, 2, 3, … n-1, and the number of stacked MOSFETs inside the dotted line is depend on i and is given by i – 1.

From (3), the every output voltage $\sim V_i$ under the MOS switch turns on are different one and another. Therefore logic regenerators are required to reshape them. In order to realize it, the common source circuit is used as the logic regenerator block. Therefore, the output voltage is reshaped and inverted and can be given by

$$V_i \approx \begin{cases} V_{dd} & \sim V_i < V_{dd} - |V_{Tp}| \\ V_{ss} & \sim V_i \geq V_{dd} - |V_{Tp}| \end{cases} \tag{4}$$

where $|V_{Tp}|$ is the threshold voltage of the PMOSFETs in the logic regenerator block. From (3) and (4), the correlation between V_i and V_{in} is given by

$$V_i = \begin{cases} V_{ss} & V_{in} < i \cdot V_T \\ V_{dd} & V_{in} \geq i \cdot V_T \end{cases} \quad (5)$$

From (5), we can find that each logic output V_i has a different threshold voltage, depending on each logic level i. Therefore we can expect that the threshold detector and logic regenerators are theoretically work for MVL circuit.

Next, we discuss about the limitation of the proposed circuit. The final output (5) will be theoretically true if;

$$V_{dd} > (i-1) \cdot V_T + \left| V_{Tp} \right| \quad (6)$$

The condition (6) is taken effect in all MVL level i in common source circuit. Since the unit logic range (V_{range}), which $i = n$-1, is given by

$$V_{range} = \frac{V_{dd}}{n-1} = V_{dd} - (i-1)V_T \quad (7)$$

Furthermore, the following condition is necessary in order to work the logic generator block.

$$V_{range} > \left| V_{Tp} \right| \quad (8)$$

It is obvious that from (6)-(8), the maximum value of MVL level "n" in proposed circuit can be determined by value of supply voltage (V_{dd}) and threshold voltage of all transistors.

B. EXPANDABLE MULTI-LEVEL GENERATOR

The multi-level generator is designed to combine MVL regenerator output (V_i) into single MVL output (V_{out}). Fig. 3 shows the circuit schematic of the proposed multi-level generator.

NMOSFETs M_{31}, M_{32}, M_{33}, and $M_{3(n-1)}$ are operate as switches. The MOS switches are controlled by the output of the MVL threshold detector, V_i {i = 1, 2, 3, …,n-1} shown in Fig.2, and selected and connected into the number of stacked MOSFETs individually. The MOSFETs M_{42}, M_{43}, and $M_{4(n-1)}$ are designed with same W and L, the MOSFETs work as V_{gs} generator. The V_{gs} can be set by I_{b3} and W/L of MOSFETs and given by

$$V_{gs} = \sqrt{\frac{I_{b3}}{K_0}\frac{L}{W}} + V_T \quad (9)$$

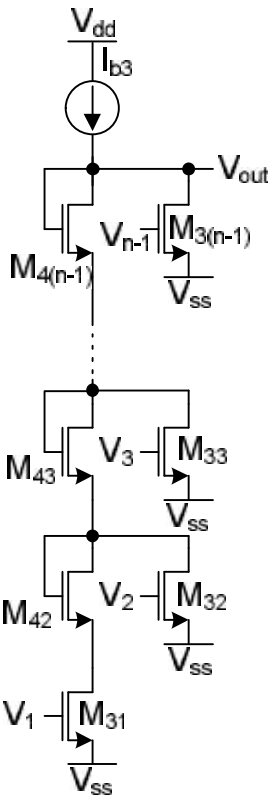

Figure 3. Circuit schematic of the proposed expandable multi-level generator

In the even if all outputs of the MVL threshold detector are V_{ss}, (V_{in}<V_T), V_{out} will be equal to V_{dd}. When only V_1 is V_{dd}, ($2V_T$>V_{in}>V_T), M_{31} turns "on" condition, cause I_{b3} flows through $M_{4(n-1)}$, …, M_{43}, and M_{42}, and V_{out} becomes equal to (n-2)V_{gs}. Moreover, when V_1 and V_2 are V_{dd}, ($3V_T$>V_{in}> $2V_T$), V_{out} becomes equal to (n-3)V_{gs}. As the results, the general form of V_{out} can be derived as follows.

$$V_{out} = (n-1-i)V_{gs} \quad (10)$$

where i=0, 1, 2, 3, …, n-1.

Next, we discuss about V_{range} of the multi-level generator. Since the maximum voltage of V_{out} is V_{dd}, V_{range} of the circuit can be given by

$$V_{range} = V_{gs} = \frac{V_{dd}}{n-1} \quad (11)$$

From (9) and (11), I_{b3} should be chosen in consideration of the noise margin.

3. SIMULATION RESULT

The proposed MVL inverter was evaluated using HSPICE with 1-poly, 5-metal, 3-well 0.18 μm CMOS process parameters. In this simulation, the quaternary inverter (n= 4) shown in Fig. 4 is selected. V_{dd} = 1.8V and V_{ss} = 0V were used in this simulation.

Fig. 5 (a) and (b) show the simulation results of the DC and transient analyses, respectively. From these figures, it can be seen that the proposed circuit operate as the quaternary inverter. Fig. 6 shows the simulation results of the pulse response. From this simulation results, the time propagation delays, rise time (t_r) and fall time (t_f) were measured. Its results are listed in Table 1 and Table 2. From these tables, the rise time and rise delay and t_r are larger than the fall delay and t_f, in all cases. These depend on the values of I_b, I_{b2}, and I_{b3}. That is to say, the relationship between the delay times and power consumption is trade-off.

4. INVERTED MVL HYSTERESIS COMPARATOR

In this Section, MVL hysteresis comparator is proposed as the application of the proposed MVL inverter.

The different between inverted MVL hysteresis comparator and the MVL inverter is the threshold-skipping effect [8]. The ideal characteristics of the inverted quaternary hysteresis comparator are shown in Fig. 7. In the inverted quaternary hysteresis comparator, 6 threshold voltages are required;$V_{0.5-}$, $V_{0.5+}$, $V_{1.5-}$, $V_{1.5+}$, $V_{2.5-}$, and $V_{2.5+}$ as shown in Fig. 7, while only 3 threshold voltages ($V_{0.5}$,$V_{1.5}$, $V_{2.5}$) are required in the quaternary inverter.

A. Hysteresis MVL Threshold Comparator Circuit 1

In the past, the current-mode inverted hysteresis comparator was proposed [9]. In the circuit, ΔI, which is difference between the rise threshold value and fall threshold value, is created in the comparator to produce hysteresis on current mode DC transfer characteristic [9]. On the other hand, the proposed quaternary hysteresis comparator (circuit 1) is use voltage-mode and is implemented by using the back gate schemes in order to applied ΔV. It is well known that V_T depends on the back gate voltage, and is called body effect. The V_T including the body effect is given by

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{sb}|} - \sqrt{|2\phi_F|}) \qquad (12)$$

TABLE I. TIME DELAY CHARACTERISTIC

Time delay (ns)		Vo(t+1)			
		0	1	2	3
Vo(t)	0		18.82	30.19	33.24
	1	3.93		25.08	33.07
	2	4.01	3.61		25.99
	3	3.84	3.69	3.01	

18.82ns is time delay on output node to change from logic 0 to logic 1.

TABLE II. RISE TIME AND FALL TIME

t_r(ns) / t_f(ns)		Vo(t+1)			
		0	1	2	3
Vo(t)	0		3.32	17.33	18.17
	1	2.25		5.33	11.64
	2	2.26	1.29		12.42
	3	2.53	1.28	0.87	

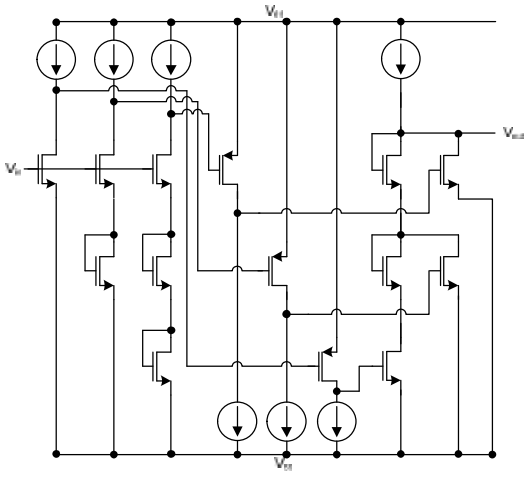

Figure 4. Quartenary MVL inverter circuit

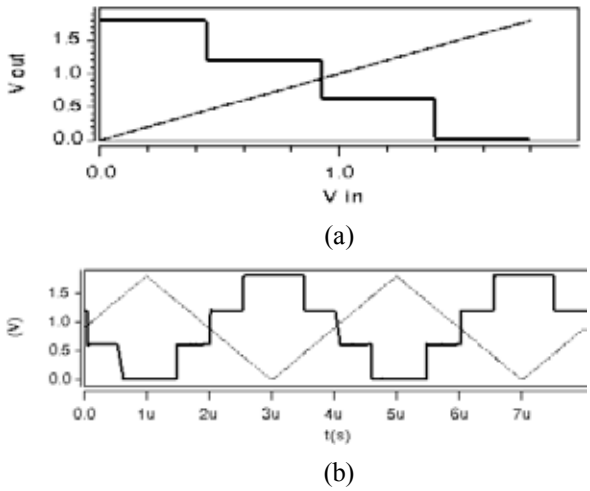

Figure 5. Quartenary MVL inverter simulation, (a) DC transfer characterisitc, (b) Transient output

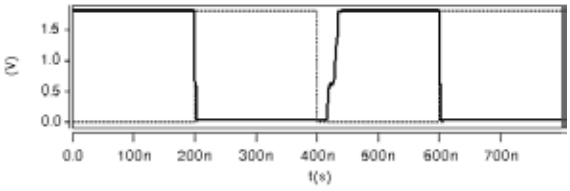

Figure 6. Switching time simulation result in fall-time and rise-time

where V_{T0} is the zero bias threshold voltage, γ is the body effect coefficient, ϕ_f is Fermi potential and V_{sb} is the source-to-back gate voltage.

In (5), the threshold voltage V_i are equal to iV_T, give a round number of V_T as threshold. In the even if one of MOSFET in iV_T is applied with the body effect, the threshold voltage is:

$$V_i = \begin{cases} V_{ss} & V_{in} < (i-1)V_{T0} + V_T \\ V_{dd} & V_{in} \geq (i-1)V_{T0} + V_T \end{cases} \quad (13)$$

Feedback scheme are used to combine (5) and (13) to produce ΔV (ΔV_T). In Fig.8, the feedback scheme and the body effect are applied in M_1, M_{51}, and M_{53} to give the different threshold voltage when V_{in} is rising and falling. The threshold voltage (V_{th}) of the inverted quaternary hysteresis comparator shown in Fig. 8 is given by:

$$V_{th} = \begin{cases} i \cdot V_{T0} & V_{in} = Rising \\ (i-1)V_{T0} + V_T & V_{in} = Falling \end{cases} \quad (14)$$

where $V_{T0} > V_T$ because V_{sb} is negative value.

The transistors M_{71}, M_{72} and M_{73} are used as V_{gs} generator to simplify control ΔV_T by V_{1L}, V_{2L} and V_{3L}.

B. Hysteresis MVL Threshold Comparator Circuit 2

The proposed quaternary hysteresis comparator (circuit 2) is use switch scheme in order to applied ΔV. The switch scheme is used to supply different value of I_b as shown in Fig. 9 to produce hysteresis characteristic. The switching characteristic is given by:

$$I_{ds} = \begin{cases} I_{b1iHIGH} & V_{in} = Rising \\ I_{b1iLOW} & V_{in} = Falling \end{cases} \quad (15)$$

where the value of $I_{b1i\,HIGH}$ is larger than $I_{b1i\,LOW}$.

Since the value of I_b is changing all over the time, the equation (5) is no longer applied, however the threshold voltage will given by:

$$V_i = \begin{cases} V_{ss} & V_{in} < i \cdot V_{gs} \\ V_{dd} & V_{in} \geq i \cdot V_{gs} \end{cases} \quad (16)$$

where the value of V_{gs} will changing depend on I_b as shown in (1) and (15), therefore the ΔV as hysteresis characteristic will occur

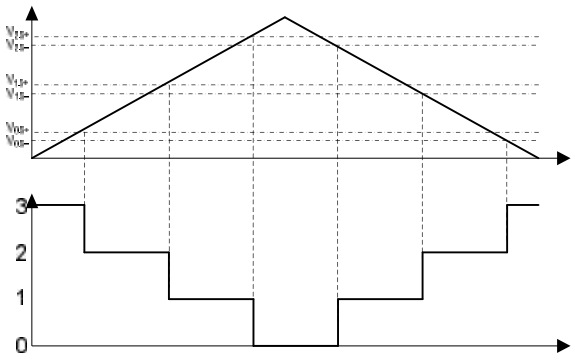

Figure 7. Proposed inverted MVL hysteresis comparator DC transfer characteristic

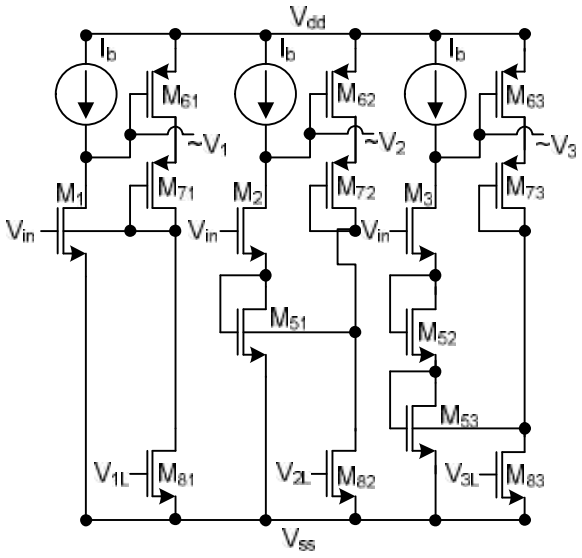

Figure 8. Proposed hysteresis MVL threshold detector with back gate scheme in M_1, M_{51}, and M_{53}.

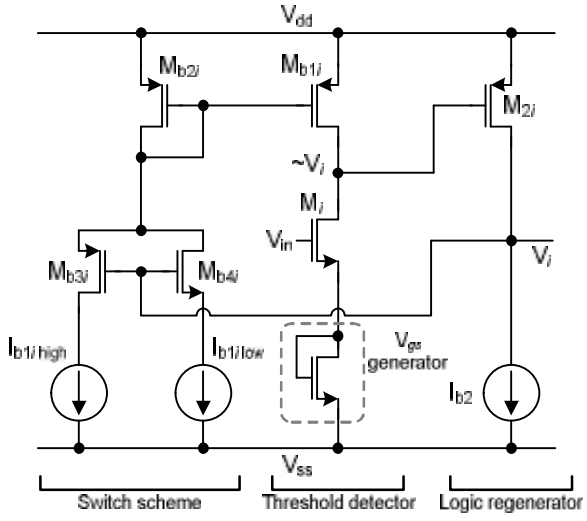

Figure 9. Proposed hysteresis MVL threshold detector with switch scheme in I_b

.

C. *Inverted MVL Hysteresis Comparator Simulation Result*

The inverted quaternary MVL hysteresis comparator was also evaluated through HSPICE with 0.18 μm CMOS process. The supply voltage V_{dd} of 1.8V was used in this simulation.

Fig. 10 shows the simulation results of the DC analysis. From Fig. 10, we can confirm that the proposed circuit operates as the inverted quaternary hysteresis comparator. Furthermore, each ΔV_T ($\Delta V_{T0.5}$, $\Delta V_{T1.5}$, $\Delta V_{T2.5}$) can be controlled by V_{1L}, V_{2L}, and V_{3L} for proposed circuit 1 and by $I_{b11\ HIGH}$ - $I_{b11\ LOW}$, $I_{b12\ HIGH}$ - $I_{b12\ LOW}$, and $I_{b13\ HIGH}$ - $I_{b13\ LOW}$ for proposed circuit 2 respectively.

The limitation of proposed MVL hysteresis comparator circuit 1 is base on V_{sb}. Since V_{sb} is a negative value, $|V_{sb}|$ cannot larger than the built in potential (0.7V in the case of silicon), or the diode connection between the source and the bulk in NMOSFET will be forward biased, and small current will flow through back gate. This issue did not occur on proposed MVL hysteresis comparator circuit 2.

5. CONCLUSIONS

In this paper, we have been proposed the new MVL inverter compatible standard CMOS process. The circuit is divided two circuit blocks: MVL threshold detector block and logic regenerator block. Next, we proposed the inverted MVL hysteresis comparator as the application of the proposed MVL inverter. The performances of the proposed MVL inverter and MVL hysteresis comparator were evaluated through HSPICE with the set of 0.18μm CMOS process parameters. From simulation results, we could confirm that the all proposed circuits operate well theoretically.

ACKNOWLEDMENT

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc. and Cadence Design Systems, Inc. I would like to thank to all staff of the University of Miyazaki and University of Brawijaya, for giving the chance to study and research at University of Miyazaki.

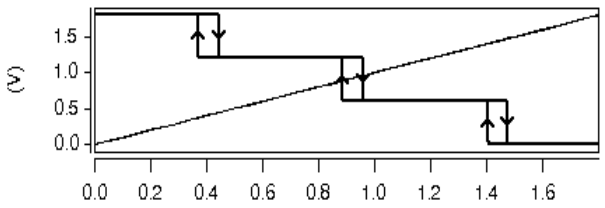

Figure 10. Inverted quartenary MVL hysteresis comparator DC transfer characterisitc

REFERENCES

[1] J. Nunez, J.M. Quintana, M.J. Avedillo, “Limits to a Correct Operation in RTD-Based Ternary Inverters,” IEEE International Symposium on Circuits and Systems (ISCAS 2008), pp. 604-607, 2008.

[2] J. Nunez, J.M. Quintana, M.J. Avedillo, “Limits to a Correct Evaluation in RTD-Based Ternary Inverters,” IEEE International Symposium on Circuits and Systems (ISCAS 2006), pp. 403-406, 2006.

[3] M. Inaba, K. Tanno, O. Ishizuka, “Analog Inverter with Neuron-MOS Transistor and Its Application,” IEICE Trans. Fundamentals. Vol.E85-A, No. 2, pp. 360-365, Feb. 2002.

[4] Y. Berg, O. Naess, S. Aunet, M. Hovin, “A Novel Floating-Gate Multiple-Valued Signal to Binary Signal Converter,” International Conference on Electronics, Circuits and Systems (ICECS 2002), Vol. 2, pp. 575-578, 2002.

[5] Y. Berg, O. Naess, S. Aunet, R. Jensen, M. Hovin, “Novel Floating-Gate Multiple-Valued Signal to Binary Signal Converter for Multiple-Valued CMOS Logic,” International Conference on Electronics, Circuits and Systems (ICECS 2002), Vol. 5, pp. V-385 – V-388, 2002.

[6] I. Thoidis, D. Soudris, I. Karafyllidis, A. Thanailakis, T. Stouraitis, “Design Methodology of Multiple-Valued Logic Voltage-Mode Storage Circuits,” International Conference on Electronics, Circuits and Systems (ICECS 1998), Vol. 2, pp. 125 – 128, 1998.

[7] M.S.E. Sendi, M. Sharifkhani. A.M. Sodagar, “CMOS-Compatible Structure for Voltage-Mode Multiple-Valued Logic Circuits,”18th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2011), pp. 438-441, 2011.

[8] X. Wu, P. Wang, and Y. Xia, “Design of Ternary Schmitt Triggers Based on Its Sequential Characteristics,” IEEE International Symposium on Multiple-Valued Logic (ISMVL 2002), pp. 156-160, 2002.

[9] K. W. Current, “Current-Mode CMOS Multiple-valued Logic Circuits,” IEEE Journal of Solid-State Circuits, Vol. 29, No. 2, pp. 95-107, Feb. 1994.